Silicon Photonic Read-Only Memory

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***Abstract*—In this paper, a CMOS-compatible in-plane micrometer-size optically readable nonvolatile-memory device is proposed and analyzed. It consists of an electrically erasable programmable read-only memory (EEPROM) integrated on a high-index-contrast silicon-on-insulator (SOI) rib waveguide. Our calculations indicate that variations on the order of 10^{-4} of the waveguide effective refractive index can be achieved for the typical values of stored charge (on the order of 10^{12} q_e/cm^2) on a floating gate. A microring resonator, based on such waveguide, efficiently converts the calculated index variations into strong intensity variations. This photonic structure can be used to create nonvolatile optically readable memory states in a photonic device [photonic EEPROM (PEEPROM)] with an ultrafast read time. A microring-resonator intensity-modulator PEEPROM is predicted to exhibit a modulation depth of 91% (10.4 dB) between the uncharged and charged (3.75×10^{12} q_e/cm^2) states. The read time of the device is only 9 ps, which is at least two orders of magnitude shorter than that of a standard two-transistor electrically readable EEPROM.**

***Index Terms*—Device modeling, integrated optics, optical memory, plasma dispersion effect, silicon optoelectronics.**

I. Introduction

SILICON as photonic material has remarkable properties. It is transparent in the range of optical-telecommunications wavelengths (1.3 and 1.55 μm) and has a high index of refraction, which permits the fabrication of high-index-contrast submicrometer structures [1]. In addition, the mature Si microelectronics [bipolar or complementary metal-oxide semiconductor (CMOS)] technology enables the implementation of dense silicon-based integrated systems on chips. Silicon-on-insulator (SOI) strip waveguide technology has been shown to be an ideal platform to achieve compact (submicrometer size) photonic devices [2]. The use of crystalline Si, instead of polysilicon or amorphous Si, as the waveguide core reduces scattering and absorption losses [2].

Relevant breakthroughs in Si photonics have been recently achieved. Laser emission [3], high-speed all-optical [4] and electrooptical [5], [6] modulations, and optical bistability [7] have been demonstrated on SOI. These active devices, besides the already demonstrated photonic passive structures such as bends, splitters, couplers, and filters [2], [8], [9], constitute the basic building blocks for the implementation of all-Si integrated photonic and optoelectronic circuits. However, scarce work has been devoted to photonic devices for permanent data storage, despite the fact that optical memory is a technology that is expected to replace the electrical data buffers in the optical-communication systems, permitting the elimination of the optical-to-electrical conversion hardware. In addition, optical methods to read memory devices would drastically reduce the read time as compared to the electronic methods, since no electrical parasitics are involved. Thus, the development of a semipermanent or nonvolatile-memory photonic device appears to be the next step for increasing the functionality and the range of applications of microphotonic circuits.

A significant achievement in the field of on-chip optically read memory devices has been the recent demonstration of a Si-nanocrystals (Si-nc)-based nonvolatile Si optical-memory device [10]. This device, which is electrically programmed and erased, is optically read. However, the reading is done in an out-of-plane geometry by monitoring the photoluminescence intensity emitted from the charged/uncharged Si-nc. In-plane optical reading through integrated waveguides would be desirable in order to achieve planar integration of memory cells with memory-location-addressing elements such as photonic wires, splitters, and all-optical routers [4] on the same Si chip.

Here, we propose an electrically erasable programmable read-only memory (EEPROM) structure integrated on a high-index-contrast SOI waveguide. An EEPROM is a conventional metal-oxide-semiconductor field-effect transistor (MOSFET) modified so that a semipermanent charge storage inside a floating gate is possible (retention time can be over years). In a previous work [11], we proposed a MOS configuration integrated on a SOI waveguide, where the induced charge modifies the index of refraction of the waveguide [12]. This effective index change is small, on the order of 10^{-4} [13]. Here, similarly to the study in [11], we enhance this effect on the transmission of the device by confining the light in a ring resonator. Conventional EEPROMs employ highly doped polysilicon layers surrounded by oxide as the floating gate. However, the use of such a highly doped conducting layer becomes prohibitive in a high-index-contrast SOI waveguide due to the proximity of that layer to the Si core, which results in a high overlap with the optical mode and, therefore, to high optical losses [11]. To overcome this problem, alternative nonconducting floating-gate structures such as silicon-nitride storage [14] and Si-nc storage [15] could be used.

In this paper, an oxide-nitride-oxide (ONO)-based photonic EEPROM (PEEPROM) integrated on a high-index-contrast SOI waveguide is studied. This nonvolatile memory is electrically written and erased, and it is optically read by a guided-wave probe beam at a 1.55-μm wavelength. An ONO stack is employed as the floating gate [16]. This allows for highly localized and relatively high-density (10^{13} cm^{-2}) trapping

Manuscript received April 13, 2005; revised March 20, 2006. The work of C. A. Barrios was supported by the Spanish Ministry of Education and Science under the Program "Ramón y Cajal."

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Digital Object Identifier 10.1109/JLT.2006.875964

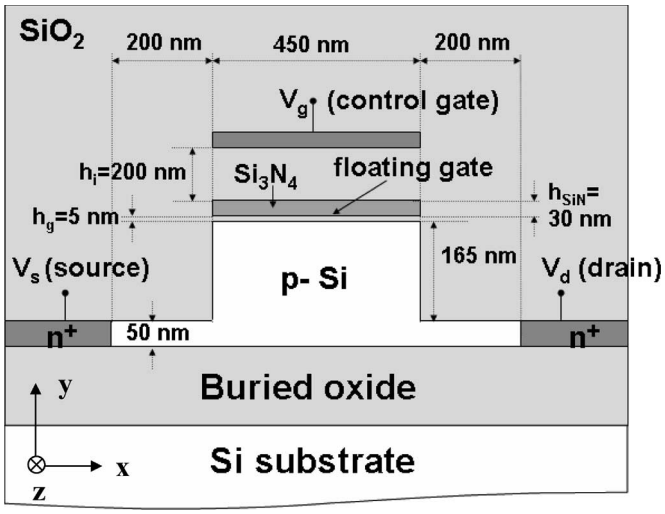

Fig. 1. Schematic cross section of an EEPROM high-index-contrast SOI rib waveguides for a 1.55-μm wavelength. Charge storage is achieved at the injection-oxide/nitride interface close to the Si core.

centers to be utilized for charge storage and avoids excessive optical losses. Section II describes the waveguide structure and the principle of operation. Section III presents the electrical and optical models. In Section IV, the results from the simulations are presented and discussed, and a PEEPROM based on a microring resonator is analyzed. Finally, conclusions are given in Section V.

II. Device Structure and Operation

Fig. 1 shows a schematic cross section of the studied EEPROM-waveguide configuration. The structure consists of a high-aspect-ratio [rib height (200 nm) $\gg$ slab height (50 nm)] rib SOI waveguide, with highly doped n-type regions $(10^{19}\ \text{cm}^{-3})$ defined in the slab at each side of the rib. The silicon layer (device layer) has a background p-type doping concentration of $10^{15}\ \text{cm}^{-3}$. The rib cross-sectional height and width dimensions are typical of a 1.55-μm-wavelength high-index-contrast strip SOI waveguide, which are 250 and 450 nm, respectively, in order to guarantee single-mode operation [11], [17]. The distance of the doped regions to the rib sidewalls is 200 nm [11], [17]. A 450-nm-wide and 30-nm-thick Si_3N_4 layer is used for the ONO-stack floating gate, whereas a 50-nm-thick and 450-nm-wide n-type highly doped $(8 \times 10^{18}\ \text{cm}^{-3})$ poly-Si layer acts as a control-gate electrode. The distance from the poly-Si control gate to the Si_3N_4 layer is 200 nm [11]. A 5-nm-thick oxide layer between the Si core and the Si_3N_4 layer will be referred to as the injection oxide, whereas the 200-nm-thick oxide between the control gate and the Si_3N_4 layer will be referred to as the control oxide. A top SiO_2 cladding layer covers the whole structure.

A practical realization of the proposed device is schematically illustrated in the abbreviated diagram of the process flow shown in Fig. 2. Conventional CMOS processes such as dry thermal oxidation and Si_3N_4 low-pressure chemical-vapor deposition (LPCVD) can be used to form a multilayer structure on a SOI wafer (Fig. 2.2). Si_3N_4 and SiO_2 layers can be etched by using reactive-ion etching (RIE) and resist as a mask. The remaining Si_3N_4 layer can be used in its turn as a mask to etch the Si device layer of the SOI platform by RIE, in order to create a rib waveguide (Fig. 2.4). Highly doped regions in the Si slab of the waveguide (Fig. 2.5) can be formed by ion implantation and annealing [6]. Then, SiO_2 can be deposited by plasma-enhanced CVD (PECVD) on the rib structure to form the control oxide (Fig. 2.6). The control gate can be fabricated by LPCVD of a highly doped poly-Si (Fig. 2.7), posterior lithography, and RIE (Fig. 2.8). The top SiO_2 cladding layer can be deposited by PECVD (Fig. 2.9). For the sake of clarity, external electrical accesses to the highly doped regions have been omitted in the diagram in Fig. 2. This can be achieved through lithography and the RIE of SiO_2. Then, ohmic contacts can be obtained by silicidation and metallization.

Charge (electrons) is added to the floating gate in order to program the memory. A drain-to-source bias voltage is applied along with a high control-gate voltage (V_{g}). The gate voltage inverts the channel, while the drain bias (V_{d}) accelerates the electrons toward the drain. Electrons can cross the thin injection oxide (5 nm) and be captured on the floating gate (defect traps at the injection-oxide/nitride interface close to the Si core) by hot carrier injection or direct tunneling [18]. When the control-gate voltage is removed, these electrons are retained in the oxide/nitride traps. The stored negative charges attract holes from the Si core to the injection-oxide/Si-core interface, creating an accumulation layer. As it occurs in a MOS configuration [11], the high concentration of holes in the accumulation layer changes the complex refractive index of Si beneath the injection oxide, through the free-carrier plasma dispersion effect [12], modifying the effective refractive index of the waveguide. This change in the index affects the transmission properties of a photonic device formed by the waveguide leading to different optical states that are determined by the amount of charge stored on the floating gate. The stored charge can be electrically erased through Fowler–Nordheim tunneling [19] by applying a negative voltage at the control gate.

III. Device Model

A. Optical Model

The beam propagation method (BPM) [20] was used for the calculation of the modal-field profile, effective refractive index, and optical losses due to carrier absorption in the waveguide. From the values of the electron and the hole concentrations at any point of the Si-core waveguide (calculated with the electrical model described below), the induced real refractive index and the optical absorption coefficient variations (Δn and $\Delta\alpha$, respectively), produced by free-carrier dispersion at a wavelength of 1.55 μm, are calculated by using [21]

$$\Delta n = \Delta n_{\text{e}} + \Delta n_{\text{h}} = -\left[8.8 \times 10^{-22} \cdot \Delta N + 8.5 \times 10^{-18} \cdot (\Delta P)^{0.8}\right] \quad (1)$$

$$\Delta \alpha = \Delta \alpha_{\text{e}} + \Delta \alpha_{\text{h}} = 8.5 \times 10^{-18} \cdot \Delta N + 6.0 \times 10^{-18} \cdot \Delta P \quad (2)$$

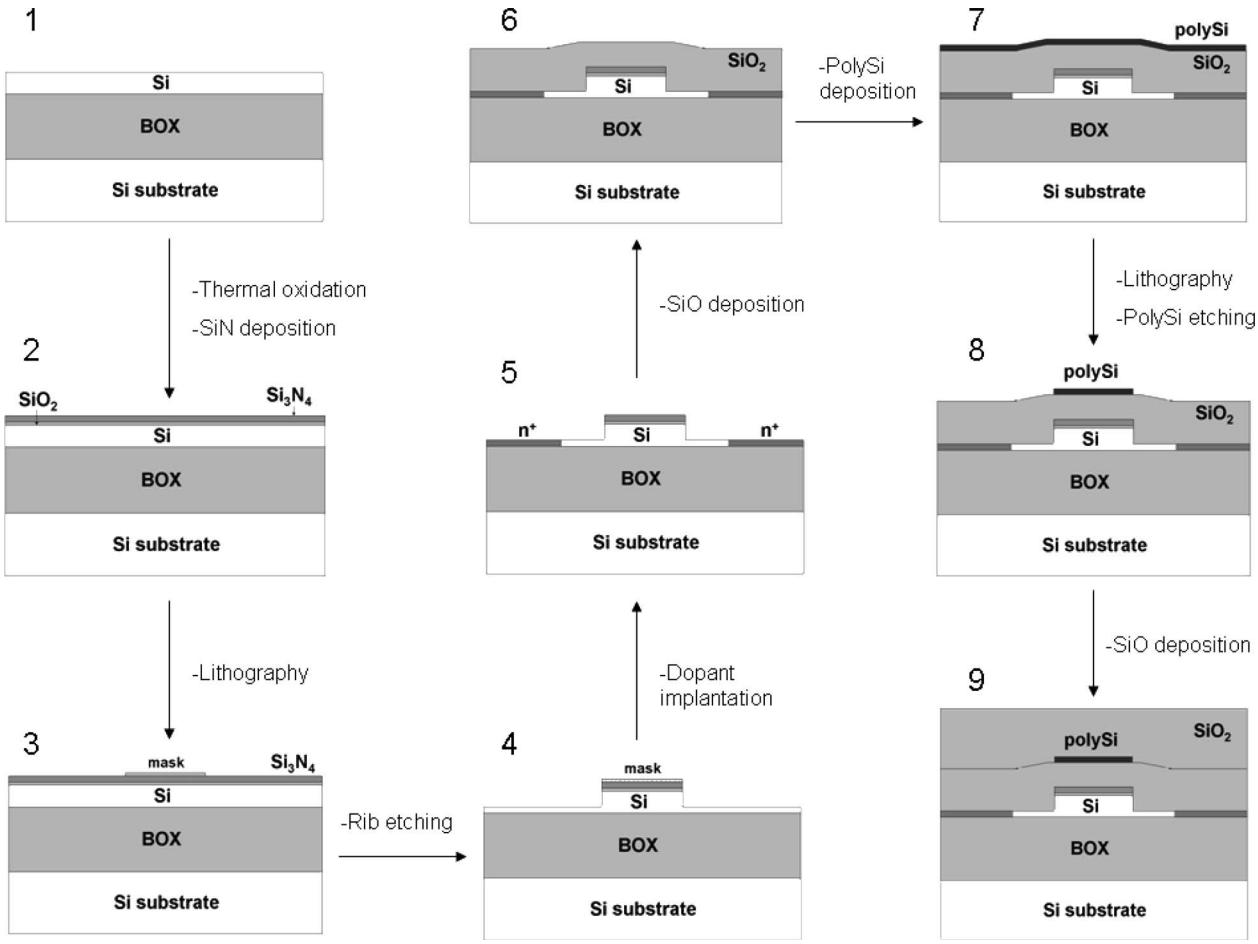

Fig. 2. Schematic process flow for the fabrication of the proposed configuration.

where

- Δn_{e} refractive-index change due to the electron-concentration change;
- Δn_{h} refractive-index change due to the hole-concentration change;
- ΔN electron-concentration change, per cubic centimeter;
- ΔP hole-concentration change, per cubic centimeter;
- $\Delta \alpha_{\mathrm{e}}$ absorption-coefficient variations due to the ΔN, per centimeter;
- $\Delta \alpha_{\mathrm{h}}$ absorption-coefficient variation due to the ΔP, per centimeter.

Equation (1) indicates that the effect on the refractive index of holes is approximately three times larger than that due to the electrons for the same carrier concentration. Equation (2) reveals that the contribution to the absorption coefficient due to the holes is lower than that due to electrons. These two facts justify the use of the hole distribution to vary the refractive index for the studied device.

B. Electrical Model

A two-dimensional (2-D) simulation package, ATLAS from SILVACO [22], was employed to achieve the electrical calculations. The suitability of this device-modeling software to analyze electrooptic devices in SOI waveguides has been demonstrated in previous works [11], [17]. This program simulates internal physics and device characteristics of semiconductor devices by solving Poisson's equation and the charge continuity equations for electrons and holes numerically. ATLAS also accounts for floating gates by using a distributed-charge boundary condition given by Gauss' law

$$Q_{\mathrm{FG}} = \int_S D ds \tag{3}$$

where Q_{FG} is the charge on the floating gate; D is the electric-displacement vector; and S represents the surface of the floating gate.

We have modeled the 2-D charge sheet, corresponding to the oxide/nitride interface close to the Si core, as a 2-D floating-gate electrode. Two main conduction mechanisms within the insulating injection-oxide layer have been considered in our model: Fowler–Nordheim tunneling [19] and hot carrier injection. In the case of the hot electron injection, the lucky electron model has been used [23].

For a given charge storage, the spatial carrier distribution in the Si core is calculated by using ATLAS and converted into a complex-refractive-index spatial distribution by employing (1) and (2). The resulting index-file distribution is exported to the aforementioned optical simulator in order to calculate the effective refractive index of the waveguide [11]. The grid

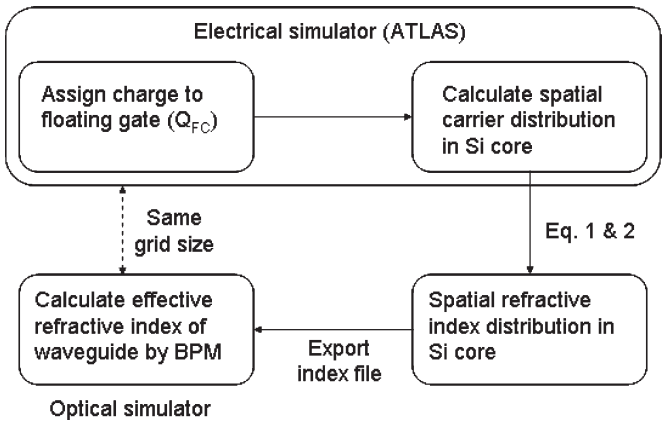

Fig. 3. Schematic diagram of the simulation procedure of the PEEPROM.

size (2 nm along the y-axis and 15 nm along the x-axis) for the simulations must be the same for both the electrical and optical calculations. The simulation procedure is schematically illustrated in Fig. 3. The surfaces of the waveguide have been considered oxide passivated. The main parameters used in the simulations are shown in Table I.

IV. Results and Discussion

In this section, the optical (optical-mode distribution, effective refractive index, and transmission losses) and electrical (programming and erasing) characteristics of the EEPROM-waveguide structure are presented and discussed. A microring resonator formed by the proposed waveguide configuration is analyzed in Section IV-C.

A. Optical Characteristics

Fig. 4 shows the fundamental transverse electric (TE)-like optical-mode distribution of the configuration shown in Fig. 1. The structure exhibits single-mode operation. The thin injection oxide does not have a significant effect on the optical characteristics of the structure, whereas the high-index nitride layer can be considered as a part of the waveguide core, contributing to the guidance of the optical mode. The highly doped regions (n^+ lateral regions and poly-Si control gate) are placed at a distance from the Si core, far enough to avoid mode overlap, which would result in excessive optical losses, but close enough to enable low-voltage operation [11], [17]. Note that a high overlap exists between the optical mode and the Si_3N_4 layer. This makes the use of a high-index material with high optical losses as a floating gate (for example, highly doped poly-Si) inappropriate.

Optical coupling from (to) an optical fiber to (from) the considered high-index-contrast rib waveguide can be efficiently achieved by using an inverse nanotaper, such as that reported in [8]. In [8], it is shown that a mode delocalization can be used in order to effectively bridge the mode and index mismatch of the index submicrometer-size waveguides and the large fibers by using compact structures.

Fig. 5 shows the carrier (hole and electron) distribution along the y-axis in the Si-core waveguide for an electron storage of 3.75×10^{12} cm^{-2} on the floating gate. As mentioned, the accumulation layer of holes formed under the injection oxide changes both the real and imaginary parts of the effective complex refractive index of the waveguide. The variation of the effective refractive index ($\Delta n_{\rm eff}$) and the optical losses of the waveguide as a function of the stored charge on the injection-oxide/nitride interface are shown in Fig. 6. $\Delta n_{\rm eff}$ is defined as the difference between the effective refractive index of the waveguide for a given charge storage and that of the uncharged ($Q_{\rm FG} = 0$) EEPROM waveguide ($n_{\rm eff,uc}$). It is seen that $|\Delta n_{\rm eff}|$ is on the order of 10^{-4} for the considered values of charge storage, which is comparable to the variations obtained in a MOS waveguide modulator [11]. As the electron storage is increased, $|\Delta n_{\rm eff}|$ increases, since the concentration of holes in the accumulation layer also increases. In addition, this induces an increment of the optical losses, as shown in Fig. 6. Note the small value of the propagation losses for the uncharged case (2.4 dB/cm), which is a consequence of the optimized position of the highly doped regions and the use of a material lossless Si_3N_4 for the floating gate. For the sake of comparison, the optical losses of the studied waveguide configuration (Fig. 1) were calculated by considering a highly doped (8×10^{18} cm^{-3}) poly-Si as the floating gate instead of the Si_3N_4 layer. Transmission losses of 31.2 dB/cm were obtained for the poly-Si floating-gate waveguide, which is ten times higher than that for the ONO stack.

B. Electrical Characteristics

Programming or writing the PEEPROM consists of two steps: 1) The first step applies a voltage ($V_{\rm g}$) to the control gate, and 2) the second step ramps the drain voltage ($V_{\rm d}$) to 5.85 V in 1 ns. Fig. 7(a) shows the transient charging curve for $V_{\rm g} = 10$ V. The calculated values of the electronic charge storage are on the typical order of magnitude (10^{12} q$_{\rm e}$/cm^2) used in conventional electronic EEPROMs. After the drain voltage is ramped, charge saturation occurs in 1 s.

Erasing the PEEPROM is achieved by grounding the control gate, disabling the drain electrode, and applying a large positive voltage ($V_{\rm s}$) at the source electrode. Fig. 7(b) shows the transient discharge for $V_{\rm s} = 100$ V and an initial stored charge of $Q_{\rm FG} = -3.75 \times 10^{12}$ q$_{\rm e}$/cm^2 on the floating gate. The charge is practically removed from the floating gate after 2 s. Lower $V_{\rm s}$ could be used, although the erasure time would increase. The difference between the erasing and programming voltages arises from the dominant conduction-current mechanism for the respective operations: Fowler–Nordheim tunneling is responsible for erasing, whereas hot electron injection is the dominant mechanism for the writing operation. One method to decrease simultaneously both the $V_{\rm s}$ and the erasure time is to illuminate the device with an ultraviolet light, as achieved in an EPROM [18].

The electric field in the injection oxide is maximum during the erasing operation, when the floating gate is uncharged. In particular, for $V_{\rm s} = 100$ V and $Q_{\rm FG} = 0$, the electric field across the injection oxide was calculated to be 4.5×10^6 V/cm, which is smaller than the dielectric strength in silicon oxide (10^7 V/cm).

TABLE I
MAIN PARAMETERS USED IN THE SIMULATIONS AT 300 K

Si refractive index, n_{Si}, (λ=1.55 μm)	3.43
n-type ($8x10^{18}$ cm^{-3}) poly-Si refractive index (λ=1.55 μm)	3.41[a]
SiO_2 refractive index, n_{SiO}, (λ=1.55 μm)	1.46
Si_3N_4 refractive index, n_{SiN}, (λ=1.55 μm)	2.0
n-type ($8x10^{18}$ cm^{-3}) poly-Si absorption coefficient (dB/cm)	352.4[b]
SiO_2 dielectric constant, ε_{SiO}, (dc)	3.9
Si_3N_4 dielectric constant, ε_{SiN}, (dc)	7.5
Electron carrier lifetime, τ_n, (ns)	50[c]
Hole carrier lifetime, τ_p, (ns)	50[c]
Si background carrier conc. (cm^{-3})	$1x10^{15}$

a) From equation (1)
b) From equation (2) and assuming undoped poly-Si absorption losses of 60 dB/cm [5]
c) From Ref. [24]

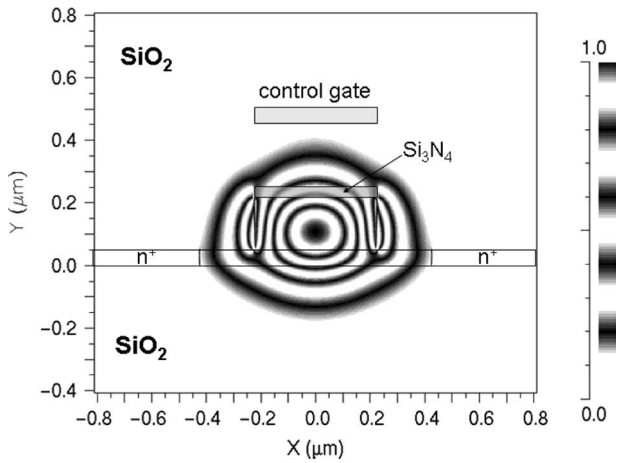

Fig. 4. TE-like fundamental optical-mode profile of the waveguide shown in Fig. 1.

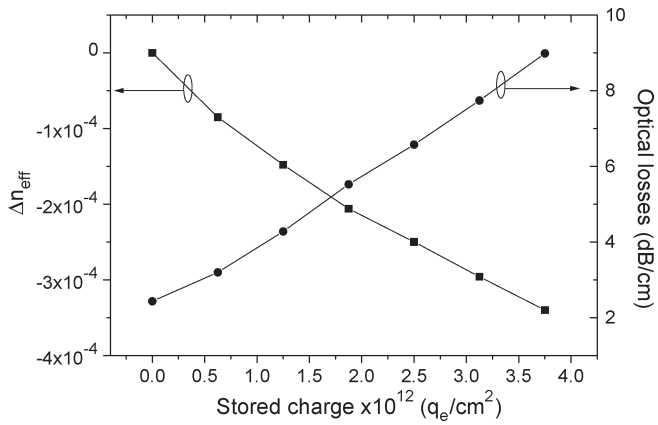

Fig. 6. Effective-refractive-index variation (squares) and optical losses (circles) of the TE-like fundamental mode as a function of the stored charge on the floating gate.

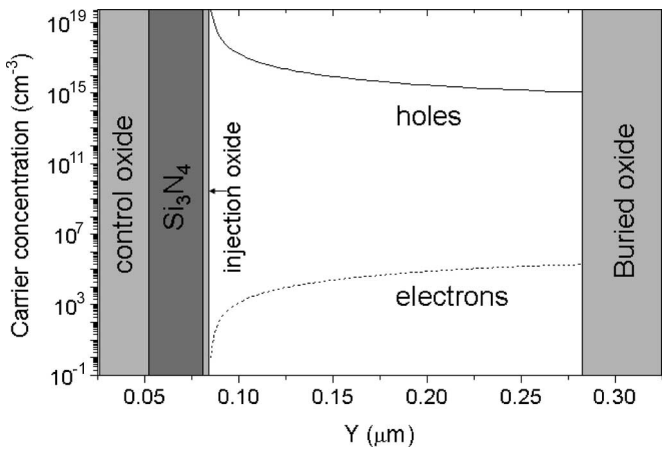

Fig. 5. Carrier distribution [holes (continuous line) and electrons (dashed line)] along the y-axis of the Si-core waveguide, when an electron surface concentration of 3.75×10^{12} cm^{-2} is stored on the floating gate.

C. Microring PEEPROM

The transmission of an optical resonator is highly sensitive to small index changes, making it ideal for intensity modulation in a short length. Thus, a waveguide intensity modulator such as a microring resonator, such as that shown in Fig. 8, can efficiently convert the small index variations calculated in the previous section into significant intensity variations. In Fig. 8, R is the radius of the ring, and d_g is the spacing between the ring and the bus waveguide (d_g is the same for both waveguide buses). The ring-waveguide structure is that shown in Fig. 1: An ONO stack is used to store charge and, as a consequence, to change the refractive index in the ring waveguide. With a proper design, the resulting phase change in the ring is converted into an output-power variation at the operation (probe) wavelength.

We estimated the output transmittivity (out port) of the microring resonator by using a matrix method [25]. Bending

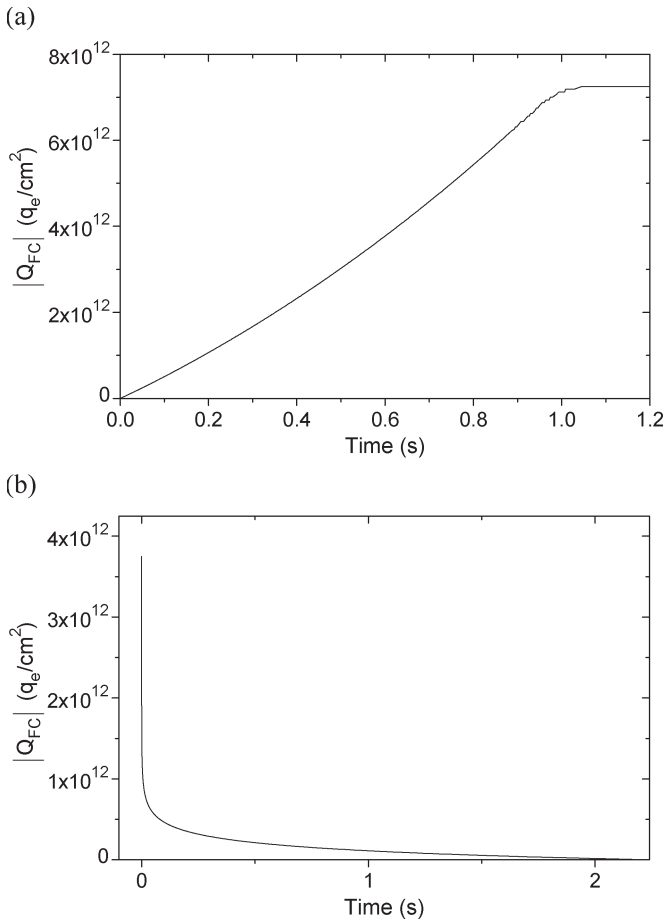

Fig. 7. Transient calculation for (a) charge storage on the floating gate (programming) for $V_{\rm g} = 10$ V and $V_{\rm d} = 5.85$ V and (b) floating-gate discharge (erasing) for $V_{\rm s} = 100$ V and initial $Q_{\rm FG} = -3.75 \times 10^{12}$ $\rm q_e/cm^2$.

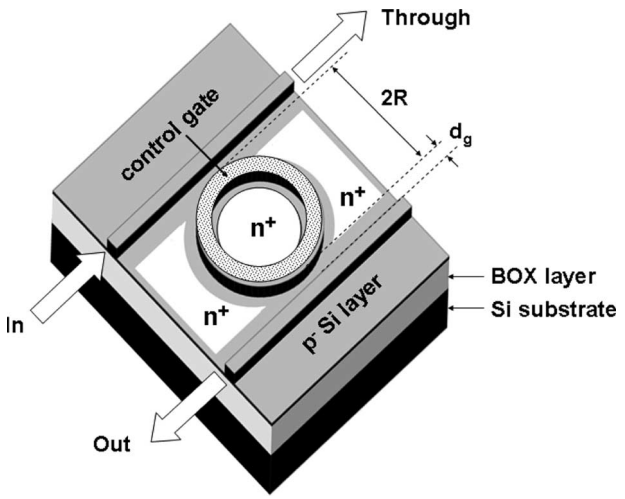

Fig. 8. High-index-contrast waveguide intensity-modulator PEEPROM based on a microring resonator. The complex refractive index of the resonant region is changed by the presence of a stored charge on the injection-oxide/nitride interface.

losses were calculated by employing the BPM [20], and the spacing between the ring and bus waveguides was estimated by using the finite-difference time-domain method (FDTD) [20]. The ring radius and the power-coupling coefficient ($|\kappa|^2$),

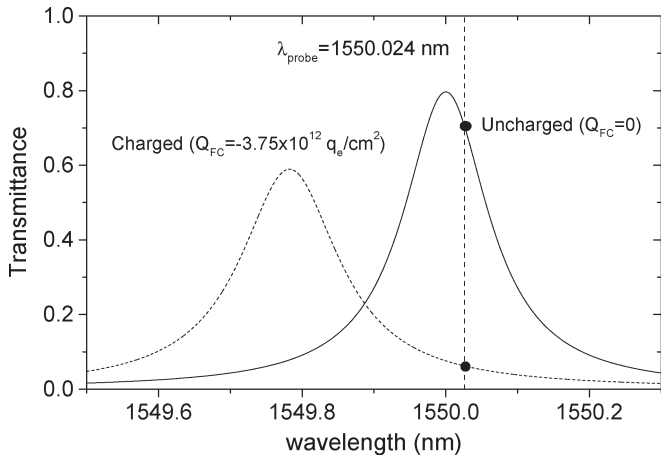

Fig. 9. Spectral transmittance (out port) for the TE-like fundamental optical mode of the simulated PEEPROM microring modulator for the uncharged state and a charged state of $Q_{\rm FG} = -3.75 \times 10^{12}$ $\rm q_e/cm^2$ for a ring radius of $R = 6.98$ μm. The circles illustrate the modulation depth at $\lambda_{\rm p} = 1550.024$ nm.

which is related to $d_{\rm g}$, determine the main resonator parameters: quality factor Q ($= \omega_0/\Delta\omega_{\rm FWHM}$, with ω_0 as the resonance frequency and $\Delta\omega_{\rm FWHM}$ as the full frequency width at half maximum), cavity lifetime $\tau_{\rm ph} (= Q/\omega_0)$, and total internal loss $A_{\rm i}$ [$= (\alpha_{\rm T} + \alpha_{\rm bend})2\pi R$, with $\alpha_{\rm T}$ as the transmission losses and $\alpha_{\rm bend}$ as the bending losses]. For optimum performance, the following are required: 1) high Q for high modulation (discrimination among different memory states); 2) small $\tau_{\rm ph}$ for short read time; and 3) low A_i for high transmittance. In order to have a resonance at the probe wavelength $\lambda_{\rm probe} = 1550$ nm, the ring radius must also satisfy the condition $2\pi R = m(\lambda_{\rm probe}/n_{\rm eff})$, where m is an integer, and $n_{\rm eff} = n_{\rm eff,uc} + \Delta n_{\rm eff}$. Here, we choose $R = 6.98$ μm and $|\kappa|^2 = 0.035$, which corresponds to a gap spacing $d_{\rm g} = 230$ nm. This results, for the uncharged state, in $Q = 1.08 \times 10^4$, $\tau_{\rm ph} = 8.9$ ps, and $A_i = 0.018$ dB ($\alpha_{\rm T} = 2.62$ dB/cm and $\alpha_{\rm bend} = 1.58$ dB/cm). For a charged state with $Q_{\rm FG} = -3.75 \times 10^{12}$ $\rm q_e/cm^2$, we obtain $Q = 9.25 \times 10^3$, $\tau_{\rm ph} = 7.6$ ps, and $A_i = 0.046$ dB.

The read time of our microring PEEPROM is determined by the resonator photon lifetime $\tau_{\rm ph}$, which are 8.9 and 7.6 ps for the uncharged and charged states, respectively. These values are at least two orders of magnitude shorter than that of a standard two-transistor electrically readable EEPROM [26].

The modulation depth (M) of the microring modulator at a given wavelength is defined as $(P_{\rm uc} - P_{\rm c})/P_{\rm uc}$, where $P_{\rm uc}$ and $P_{\rm c}$ are the transmitted output power (out port) in the "uncharged" and "charged" states, respectively. Fig. 9 shows the transmission characteristics (output port) for the designed microring ($R = 6.98$ μm and $|\kappa|^2 = 0.035$). The refractive index in the cavity is modulated between $Q_{\rm FG} = 0$ ($\Delta n_{\rm eff} = 0$, uncharged state) and $|Q_{\rm FG}| = 3.75 \times 10^{12}$ $\rm q_e/cm^2$ ($\Delta n_{\rm eff} = -3.4 \times 10^{-4}$, charged state). The modulation depth and transmittivity for the uncharged state at the probe wavelength 1550.024 nm are 91.2% (10.4 dB) and 71.4%, respectively. The calculated modulation depth at the probe wavelength as a function of the charge storage is shown in Fig. 10. It is seen that the modulation depth begins to saturate as the electron surface concentration on the floating gate increases.

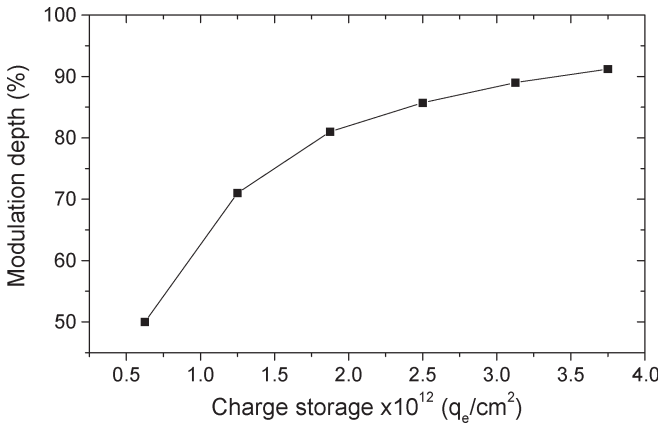

Fig. 10. Calculated modulation depth of the PEEPROM microring resonator as a function of the charge storage ($|Q_{\mathrm{FG}}|$) at $\lambda_{\mathrm{probe}} = 1550.024$ nm.

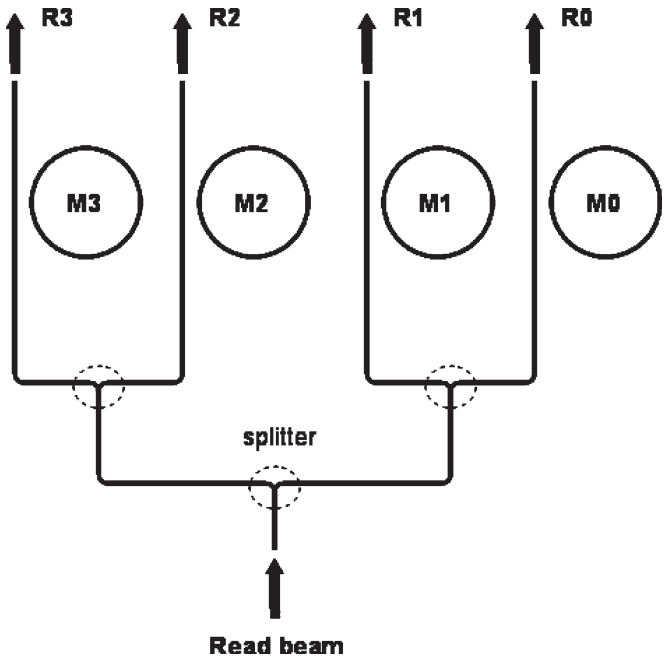

Fig. 11. Schematics diagram of a 4-bit array memory. The total insertion losses are determined by the splitter and ring losses.

Multiple rings can be integrated in order to form an array of memory elements. For this, waveguide splitting can be used, as shown schematically in Fig. 11. In this case, the total insertion losses will be determined by the splitting losses, which are expected to be on the order of 0.3 dB [27], and the previously calculated ring losses.

It must be mentioned that, due to the nonnegligible value of the thermooptic effect in Si ($\mathrm{d}n/\mathrm{d}T \approx 2 \times 10^{-4}\,\mathrm{K}^{-1}$), temperature effects on the index should be minimized in the studied configuration. This can be achieved by employing a strain silicon waveguide [28] introduced in the fabrication process by, for example, controlling the overcladding deposition conditions [29]. The introduced strain induces a decrease of the refractive index with the temperature, which counterbalances the thermooptic effect in a silicon [28].

Note, however, that the thermooptic effect can be positively used to control the phase of operation in the ring resonator. In a real device, deviations from the targeted device dimensions usually occur due to fabrication issues. This may change the designed phase in the ring resonator, leading to deviations in the spectral characteristics of the device. By using a thermocooler element as that employed in commercial DFB lasers for telecom applications, the refractive index of Si can be modified and controlled, compensating dimension deviations resulting from the device processing. If a phase control is required for a single device, local heating could be achieved by using the control gate of the device as a thermoresistor. Since the control gate is only used during the write and erase operations, it would be feasible to pass an electrical current through it (Joule effect) for the phase control during the read operation.

V. Conclusion

We have proposed and studied a PEEPROM integrated on a SOI high-index-contrast waveguide for a 1.55-μm operation wavelength. The real refractive index and the absorption coefficient of the Si-core waveguide are programmed by using the free-carrier dispersion effect (hole accumulation layer) induced by the charge storage on an ONO-based floating gate. Effective-refractive-index variations on the order of 10^{-4} are predicted for stored-charge values on the order of 10^{12} $\mathrm{q_e/cm^2}$. A 14-μm-diameter microring resonator is used to form the PEEPROM and translate these index variations into an intensity modulation depth of 91% between the charged and uncharged states. The read time of the PEEPROM is 8.9 ps, two orders of magnitude shorter than that exhibited by conventional electrically readable electronic EEPROMs, making the proposed structure very promising for the implementation of CMOS-compatible micro and nanophotonic integrated flash memory cells for ultrahigh-speed data access.

Acknowledgment

The authors would like to thank Prof. R. R. Panepucci and Dr. V. R. Almeida for their useful discussions.

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