

# Oxidized Silicon-On-Insulator (OxSOI) from bulk silicon: a new photonic platform

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**Abstract:** We demonstrate a bulk silicon alternative to the conventional silicon-on-insulator photonics platform, using common CMOS process-based Si<sub>3</sub>N<sub>4</sub> masking and oxidation techniques. We show waveguide losses as low as 2.92 dB/cm with a technique that can be implemented on the front-end of a typical CMOS fabrication line.

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## 1. Introduction

The case for silicon photonics has been made many times over. Sub-wavelength optical wires fabricated using CMOS (Complementary Metal–Oxide–Semiconductor) materials and techniques will lead the way to feasible and economic integration of optics and electronics. This in turn will open the door to high-bandwidth, low-power interconnects that can be used for applications such as chip multi-processor interconnects or low-jitter chip-wide clock distribution networks [1]. Nevertheless, there is still no consensus as to the specifics of how this integration will happen; only that it needs to happen [2, 3].

One of the main drawbacks of the integration of optics on the transistor layer is the need for extensive cladding material, typically a few micrometers of silica surrounding the silicon core waveguide. Although high-contrast optics in principle occupies small real estate, the optical wire - a typical Si channel waveguide (e.g. 450 nm wide x 250 nm thick), still requires around 1  $\mu\text{m}$  of  $\text{SiO}_2$  cladding on all sides. This optical buffer is needed mainly underneath the waveguide in order to eliminate crosstalk to the nearby substrate. In electronics however, only a small layer of  $\text{SiO}_2$  is needed. In fact, having more than a few hundred nanometers of  $\text{SiO}_2$  underneath the Si waveguide creates incompatibility with the CMOS transistor layer, which necessitates thermal conduction through the silicon substrate [4]. Modern processes which use SOI (Silicon-On-Insulator) technology rely on a "thick" silica layer around 70 nm and better transistor performance can be achieved with a 40 nm BOX (Buried Oxide) layer [5]. Yet even with older SOI CMOS stacks which rely on up to a 400 nm BOX [4], optical losses from radiation would be in the thousands of dB/cm. Comparatively from our simulations 1  $\mu\text{m}$  of BOX would lead to 0.35 dB/cm and 3  $\mu\text{m}$  would lead to negligible loss assuming chips with several centimeters of waveguides between nodes.

One option for the integration of optics with electronics is the fabrication of the optics layer in the backend of the CMOS stack, alongside the metallization layers [6], however single-crystalline silicon would not be available as a guiding material, since it cannot be deposited. In addition this approach limits fabrication to low-temperature processes, when done monolithically. Alternatively one could envision using flip-chip bonding; however this would reduce the already limited area reserved for off-chip contacts. Instead it would be preferable if the optics could be built alongside the transistor layer where high-temperature processes are allowed and close contact with electronics is maintained, allowing the architect full flexibility in design.

Here we propose a fabrication process for enabling the integration of optics on the transistor layer. The process is based on the traditional electronic medium, namely a bulk silicon wafer and produces small or non-existing BOX for the electronics while providing an optical buffer for the optics sharing the layer.

## 2. Process definition and simulation

We generate high quality oxide in bulk silicon beneath our waveguides using thermal oxidation, having protected them with a material with very high oxidation temperature and CMOS compatibility:  $\text{Si}_3\text{N}_4$ . A similar technique is used in some CMOS fabrication in a process called LOCOS (LOCAL Oxidation of Silicon), in which oxide spacers are created between transistors to avoid parasitic effects. LOCOS has been used to make waveguides, though typically they are large ridge waveguides with little confinement [7, 8]. Smith et al. have previously shown the formation of waveguides by excavating air pockets underneath waveguides made of polycrystalline silicon [9]. This process requires depositing the guiding layer since it needs a buffer layer to protect the guiding material from the silicon-etching chemical. By maintaining the original crystalline silicon above our oxide layer we ensure a high quality optical guiding medium is used.

In order to induce oxidation from beneath the waveguide in order to optically isolate the waveguide from its substrate we use a full three-sided nitride cap as a protective cover over an etched pillar that will be formed into the final waveguide (see figure. 1). In electronics a similar process is used referred to as SWAMI (SideWall Masked Isolation) and is used in some transistor fabrication [10]. Using the Silvaco modeling program Athena we simulate the oxidation growth for our waveguide structure, shown in Fig. 1. We generally find good agreement in the resulting shape of the structure in these simulations, though the simulation underestimated the oxidation time. In Fig. 1(a) the waveguide-like structure has been clad with  $\text{Si}_3\text{N}_4$  and overetched by just under 1  $\mu\text{m}$  before being subjected to oxidation. Under oxidation the structure narrows from either side (Fig. 1(b)) until it separates from the substrate at which point we can begin to see the makings of a "buried oxide layer" in Fig. 1(c). From

this point we continue to oxidize for two reasons: 1) to increase the distance from the waveguide to the substrate and 2) to reduce the triangular “tail” of the waveguide to a flat surface as seen in Fig. 1(c). Further flattening can be achieved with increased oxidation time.

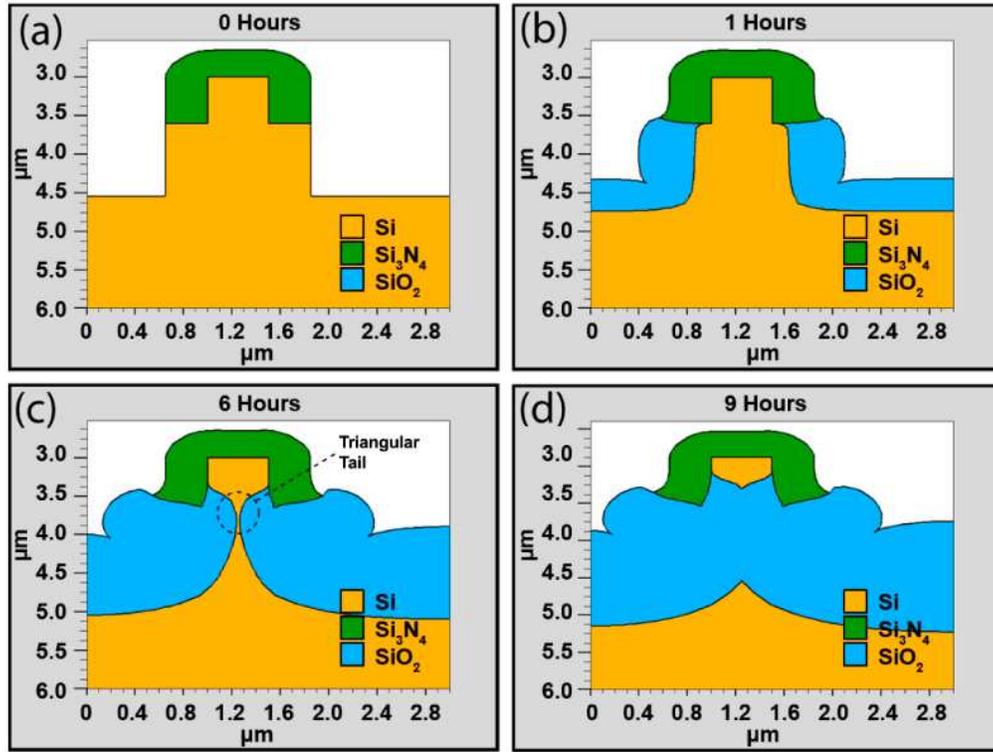


Fig. 1. Simulated effects of wet oxidation on waveguide structure: (a) post over-etching and prior to oxidation, (b) 1 hour of oxidation, (c) 6 hours of oxidation, (d) 9 hours of oxidation.

### 3. Fabrication

The fabrication process relies on a single step of lithography, deposition of  $\text{Si}_3\text{N}_4$ , etching and oxidation. We begin with a blank silicon wafer (Fig. 2(a)), on which we deposit a 300 nm layer of  $\text{Si}_3\text{N}_4$  using PECVD (Plasma-Enhanced Chemical Vapor Deposition) or LPCVD (Low-Pressure Chemical Vapor Deposition). This layer serves as the top cover of the protective mask (Fig. 2(b)).

We define the waveguide devices using a negative photo or electron-beam lithographic method resulting in a hardened resist material over the areas to be protected (Fig. 2(c)). The waveguides are defined to be 450 nm wide according with our standard geometry to maintain single-mode operation and tight bending radii [11]. These structures are etched vertically down using an ICP (Inductively-Coupled Plasma) or RIE (Reactive-Ion Etching) tool. The results of this step are waveguide-like pillars 600 nm tall with a  $\text{Si}_3\text{N}_4$  layer on top. We have made the pillars purposefully taller than the designed waveguide thickness of 250 nm since they need to be oxidized from underneath to create a flat bottom surface (Fig. 2(d)).

As a sidewall protection from the oxidation to the waveguides we deposit another 350 nm of  $\text{Si}_3\text{N}_4$  (Fig. 2(e)). The  $\text{Si}_3\text{N}_4$  layer is etched the same amount as was deposited. The verticality of the etch leaves  $\text{Si}_3\text{N}_4$  on the sidewalls of the pillars. Given the initial layer of  $\text{Si}_3\text{N}_4$  left on top we have as a result a three sided mask over all waveguiding structures (Fig. 2(f)). We refer to this step as being self-aligned, since the mask is left only over the waveguides without the need for an additional lithography step. We continue etching into the

silicon substrate to reduce the amount of oxidation time and  $\text{SiO}_2$  generated on the sides (Fig. 2(g)). This step reduces the spacing necessary between adjacent waveguides or directionally coupled devices.

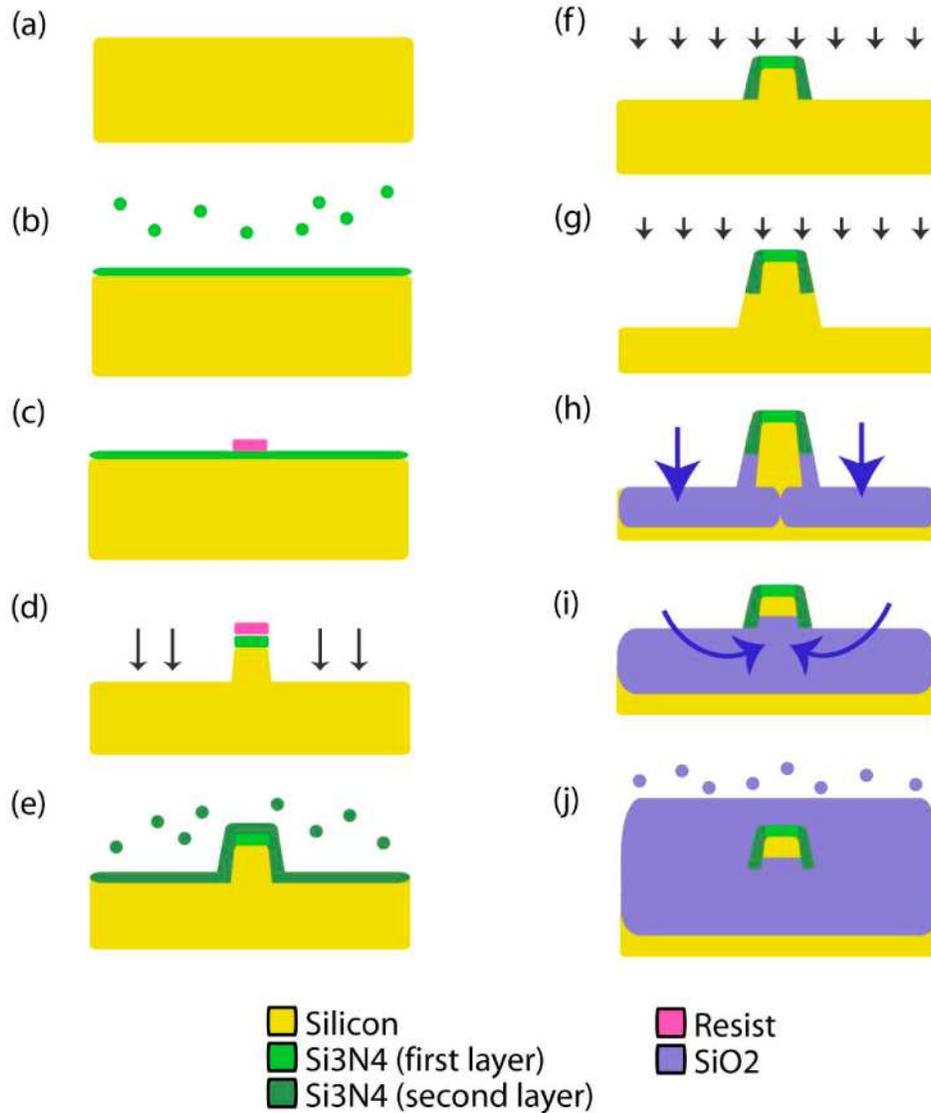


Fig. 2. Process flow: (a) bulk silicon wafer, (b)  $\text{Si}_3\text{N}_4$  deposition, (c) lithographic waveguide definition, (d) ICP etch, (e)  $\text{Si}_3\text{N}_4$  deposition, (f) ICP cap etch, (g) extended etch for quicker oxidation, (h) wet oxidation for buffer layer growth, (i) extended wet oxidation for waveguide underlayer flattening, (j) upper layer oxide deposition to complete optical buffer.

The wafer is placed in a wet oxidation chamber at  $1100^\circ\text{C}$  which grows  $\text{SiO}_2$  in the regions of exposed silicon. The  $\text{SiO}_2$  reaches underneath the structure creating the BOX layer (Fig. 2(h)). At first a triangular bottom is formed but extended oxidation into the underside of the Si pillars reduces the pinched point into a flat underside (Fig. 2(i)). At  $1100^\circ\text{C}$  the oxidation took a total of 16 hours which is a clear limitation but could be reduced considerably with a higher temperature process and by designing a narrower waveguide. The  $\text{Si}_3\text{N}_4$  layers can be removed at this point, though from our simulation it does not disturb the

mode profile and so we leave it on the waveguide. Finally the structures are clad with 3  $\mu\text{m}$  PECVD  $\text{SiO}_2$  to complete the surrounding optical buffer (Fig. 2(j)).

#### 4. Results

The overall shape of the fabricated waveguide itself is rectangular (seen in Fig. 3(a)) and provides a confined optical mode shown in Fig. 3(b), unaffected by the leftover  $\text{Si}_3\text{N}_4$ . One can see that using this process we indeed create a sizable BOX layer beneath our crystalline silicon waveguide. Figure 3(c) shows the 3.3  $\mu\text{m}$  BOX layer beneath three adjacent waveguides.

The thicknesses of the two nitride layers were determined through various trials in order to avoid over-etching (visible in the thin top corners of the  $\text{Si}_3\text{N}_4$  layer in Fig. 3(a)) that would lead to unwanted oxidation of the waveguides. The thicker cover however, coupled with the  $12^\circ$  sidewall angle produced by our ICP etcher and an additional patterning layer (150nm  $\text{SiO}_2$  hard-mask) resulted in an increase of the waveguide width. The outcome is a waveguide 740 nm wide. A smaller waveguide can be made in two ways: either writing 160 nm patterns which would result in 450 nm waveguides, or ideally using an etcher with higher verticality that would also reduce the necessary thicknesses of the two  $\text{Si}_3\text{N}_4$  layers. Given a perfectly vertical etcher the thickness of each of the  $\text{Si}_3\text{N}_4$  layers would need to be slightly over 100 nm each to provide the necessary protection for the given oxidation time [12].

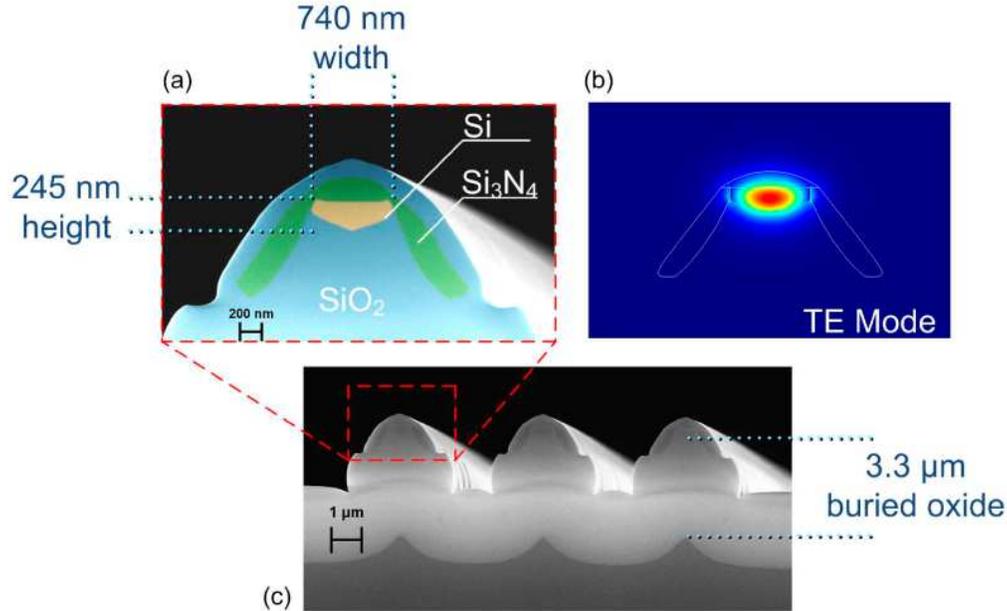


Fig. 3. Final experimental waveguide shape shown: (a) closeup false color SEM of waveguide cross-section; (b) fundamental TE mode with effective index of 2.63, TM shown for comparison; (c) SEM showing buried oxide layer.

Finally we tested the fabricated waveguides for propagation losses using the cut-back method. Fiber coupling was used to guide light at the standard telecom wavelength of 1550 nm, incident from the polished edge of the chip. Light was collected at the output edge with a collimating objective and power detector. We observed similar losses for TE and TM modes and report here on unpolarized light. We measured 2.92 dB/cm loss shown in Fig. 4. From our simulations a BOX greater than 3  $\mu\text{m}$  should result in radiation losses into the substrate of less than 0.001dB/cm. We believe the propagation losses could be significantly reduced with improved etching techniques and should be limited to single crystal silicon waveguide losses. It should be noted that a low quality PECVD  $\text{Si}_3\text{N}_4$  was used in these samples which could

result in some material absorption. This can easily be resolved through the use of LPCVD  $\text{Si}_3\text{N}_4$ .

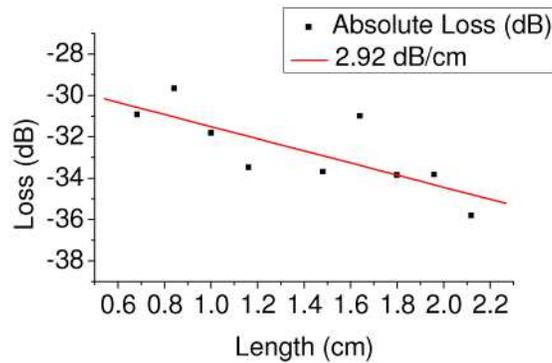


Fig. 4. Experimental loss for varying lengths of waveguide measured at 1550 nm, and loss per length fit of 2.92 dB/cm.

## 5. Conclusions

The process described in this paper produces small (sub 1  $\mu\text{m}$  width) waveguides with channel geometry, on a common bulk silicon wafer with losses of 2.92 dB/cm, comparable to those of typical SOI waveguides. The waveguides are made of single-crystalline silicon, important for maintaining high contrast guiding in small footprint devices with low losses. The optical layer is made directly on a real CMOS compatible wafer with real CMOS compatible processes, such that it can be integrated in parallel to the transistor layer of a currently fabricated electronics chip. Finally the process requires only one lithography step, thereby reducing the variability in the fabrication of both the photonic material stack as well as the devices.

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