

# Low loss etchless silicon photonic waveguides

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**Abstract:** We demonstrate low loss silicon waveguides fabricated without any silicon etching. We define the waveguides by selective oxidation which produces ultra-smooth sidewalls with width variations of 0.3 nm. The waveguides have a propagation loss of 0.3 dB/cm at 1.55  $\mu\text{m}$ . The waveguide geometry enables low bending loss of approximately 0.007 dB/bend for a 90° bend with a 50  $\mu\text{m}$  bending radius.

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**OCIS codes:** (230.3120) Integrated optics devices, (230.7370) Waveguides. (250.5300) Photonic integrated circuits.

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Low loss silicon waveguides are critical for on-chip optical networks and have been studied extensively for the past two decades. Ridge waveguides with relatively large cross sectional dimensions of 1 – 5  $\mu\text{m}$  exhibit relatively low losses down to 0.2 dB/cm [1-9]. However, the minimum bending radius of these waveguides required for low loss is large, typically 200 - 600  $\mu\text{m}$ . Strip waveguides, with relatively small cross sectional dimensions of approximately 450 x 250 nm and with small bending radius of a few microns, exhibit much higher losses - the lowest loss reported to date at  $\lambda=1.55 \mu\text{m}$  is around 1 – 2 dB/cm [10-16]. These losses, due to both scattering at the sidewalls and absorption sites at the Si/SiO<sub>2</sub> interface, originate mainly from the etching process [10,17].

In order to minimize the losses of silicon waveguides, we use an etchless process based on selective oxidation. Similar processes have been used to make ridge waveguides with losses of 0.2 – 1.0 dB/cm [7-9]. The etchless silicon waveguides are fabricated from a silicon-on-insulator (SOI) wafer with a device layer of 500 nm and a buried oxide layer (BOX) of 3  $\mu\text{m}$ . We grow a thermal oxide layer of 800 nm which consumes approximately 370 nm of silicon (Fig. 1(a)). We then pattern the waveguides with electron beam (e-beam) lithography using ma-N 2403 resist. This pattern is then transferred into the top oxide layer with reactive ion etching (RIE), where all but a thin slab of 50 nm of the SiO<sub>2</sub> is removed (Fig. 1(b)). This thin slab is left so that the silicon is never exposed to the etching plasma, therefore preventing damage from the ion bombardment and chemical reactions that occur during plasma etching. After stripping the e-beam resist, we use thermal oxidation to define the waveguide in the silicon (Fig. 1(c)). Lastly, the waveguides are clad with 2.5  $\mu\text{m}$  of plasma enhanced chemical vapor deposition (PECVD) SiO<sub>2</sub> (Fig 1(d)) and annealed at 1100°C for 3 hours to densify the film and drive out gaseous byproducts introduced during deposition. Note that in the process flow, only the top oxide layer is etched while the core waveguide is not. We fabricate etchless waveguides of both 1 and 1.5  $\mu\text{m}$  widths as defined during lithography. A waveguide that is patterned at 1  $\mu\text{m}$  width supports only the fundamental quasi-TE (x-polarized) mode, shown in Fig. 2, and no quasi-TM (y-polarized) modes. On the other hand, the 1.5  $\mu\text{m}$  wide waveguide supports higher order modes. For each waveguide width, we fabricate seven replicates of three different waveguide lengths arranged in a paper clip pattern, in order to account for variation in the fabrication process.

The resulting waveguides patterned at 1  $\mu\text{m}$  and 1.5  $\mu\text{m}$  width are 70 nm thick and 90 nm thick, respectively, and are relatively highly confining. The etchless waveguide dimensions are designed using Silvaco Athena for calculating the core profile and a finite difference mode solver for calculating the supported modes. We simulate the oxidized waveguide profile for waveguides 1  $\mu\text{m}$  (see Fig. 1(c)) and 1.5  $\mu\text{m}$  wide. We then import the simulated profiles into the finite difference mode solver and calculate the supported modes. One can see from Fig. 2 that the 1  $\mu\text{m}$  waveguide has a mode with cross sectional dimensions of 1.01  $\mu\text{m}$  by 0.52  $\mu\text{m}$  (measured at the 1/e field decay point). For comparison the fundamental mode of a typical 450 nm x 250 nm silicon strip waveguide has cross sectional dimensions of 0.37  $\mu\text{m}$  by 0.35  $\mu\text{m}$ . The confinement factor  $\Gamma$  is defined as [18]:

$$\Gamma = \frac{n_A c \epsilon_o \iint_A |\vec{E}|^2 dx dy}{\iint_{\infty} \text{Re}\{\vec{E} \times \vec{H}^*\} \cdot \hat{e}_z dx dy}, \quad (1)$$

where  $n_A$  is the core index. For the 1  $\mu\text{m}$  etchless waveguide the confinement factor is 0.38. One should note that this factor is only three times smaller than the confinement of a typical oxide clad, 450 nm by 250 nm silicon strip waveguide ( $\Gamma=1.1$ ).

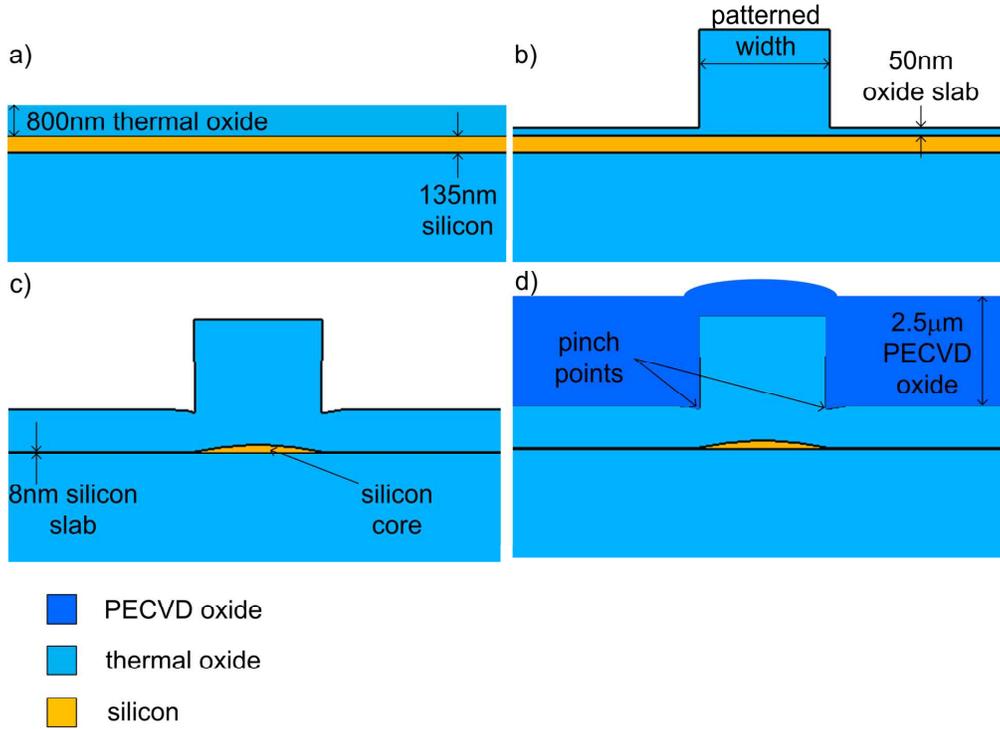


Fig. 1. Fabrication process for the etchless waveguides. a) 800 nm of thermal oxide are grown on an SOI wafer with a 3  $\mu\text{m}$  buried oxide. b) Waveguides are patterned with e-beam lithography and the oxide is etched. c) Waveguide core is defined using thermal oxidation. d) PECVD oxide is deposited as an overcladding.

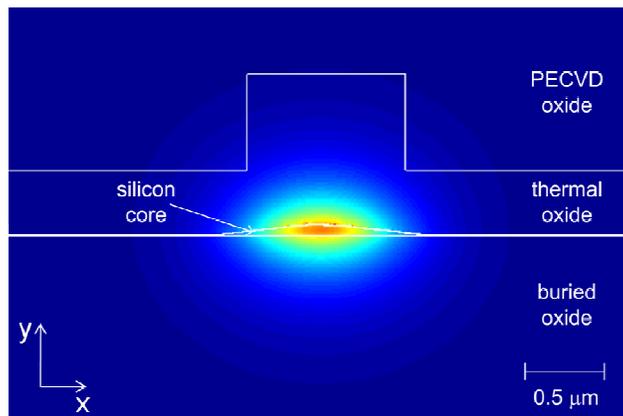


Fig. 2. TE mode profile for 1  $\mu\text{m}$  wide etchless waveguide with cladding profile.

The waveguide cross-section shows a continuous profile with a smooth, discontinuity-free transition between the thickest (center) and thinnest (either sides) parts of the waveguide, as is evidenced from the measurements and simulations (see Fig. 3). In addition, the oxidized surface of the silicon core is extremely smooth. Fig. 4(a) shows an AFM scan of a 1.5  $\mu\text{m}$  waveguide which reveals that any sidewall roughness transferred during the oxide RIE etch is not present in the silicon core. On the slab surface, the roughness, measured over a 1  $\mu\text{m}$  by 1  $\mu\text{m}$  area, is 0.3 nm RMS. For comparison Fig. 4(b) shows an AFM scan of an etched strip waveguide with typical losses of 3 dB/cm where one can see much higher sidewall roughness.



Fig. 3. Cross-section SEM image of an etchless waveguide.

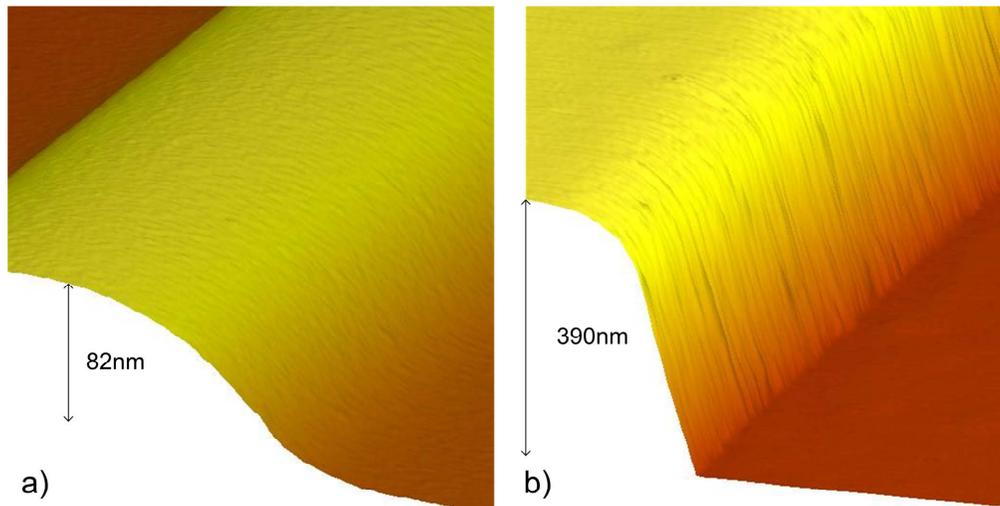


Fig. 4. (a) AFM scan of an etchless waveguide core. Original pattern width was 1.5  $\mu\text{m}$ . (b) AFM scan of strip waveguide with typical losses of 3 dB/cm.

We measure the losses of the etchless waveguides to be as low as 0.3 dB/cm. We test the waveguides using an amplified spontaneous emission (ASE) source with a wavelength centered at 1520 nm. The output of the ASE source, following a polarizer and a polarization controller, is coupled into the waveguides via a single mode tapered fiber. The output of the waveguides is then sent through a polarizer and focused onto a detector. In Fig. 5 one can see the measured output of the waveguides as a function of their lengths. We measure  $0.3 \pm 0.02$  dB/cm loss for 1  $\mu\text{m}$  wide etchless waveguides operating in the TE mode. The 1.5  $\mu\text{m}$  wide waveguide shows losses of  $0.5 \pm 0.05$  dB/cm. We suspect that the difference in loss is due to e-beam stitching errors in the wider waveguide during fabrication. Fiber coupling to these waveguides can be maximized by using nanotapers [19] to enhance the coupling efficiency.

The 1  $\mu\text{m}$  etchless waveguide only supports quasi-TE polarization. When TM polarization was launched, no guiding was observed. On the other hand, when TE polarization was launched, we measured a TE to TM extinction ratio at the output greater than 25dB confirming that the polarization state is maintained during propagation.

The observed waveguide losses can be attributed to imperfections in the upper cladding and to the field interaction at the silicon/silicon oxide interface. The PECVD oxide overcoat is not perfectly conformal and small voids may form in the pinch points (shown by the arrows in Fig. 1(d)) from the thermal oxidation mask and cause scattering losses. Additionally, impurities in the upper cladding may cause absorption. Finally, the upper and lower silicon/silicon oxide interfaces could be causing some of the observed losses through surface states absorption [17].

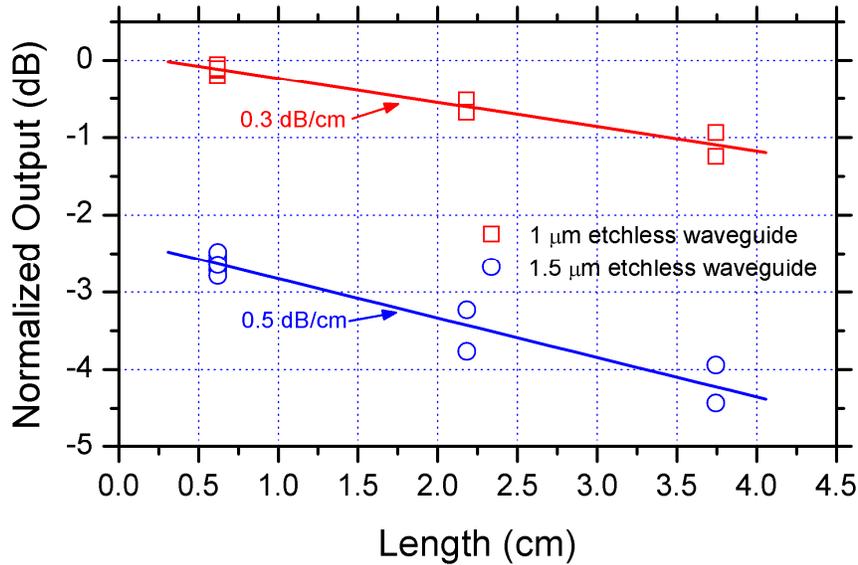


Fig. 5. Measurement results for etchless waveguides. We measured losses of 0.3 dB/cm for a 1  $\mu\text{m}$  waveguide and 0.5 dB/cm for a 1.5  $\mu\text{m}$  waveguide for the TE mode. Each marker denotes a measurement for a different waveguide on the same chip. The solid lines are the linear fit to the experimental data. The output is normalized relative to -16.1 dBm.

The etchless waveguides require a minimum bending radius only approximately ten times larger than the one of traditional highly confined strip waveguides [20]. In Fig. 6 we show the measured bending losses for the 1  $\mu\text{m}$  etchless waveguides. The uncertainty in the measurement is 0.005 dB/bend. As one can see, the etchless waveguide has negligible losses for a bending radius of 50  $\mu\text{m}$ . Similar bending losses can be achieved with ridge waveguides using a much larger bending radius of a few hundreds of microns [5 - 6, 9].

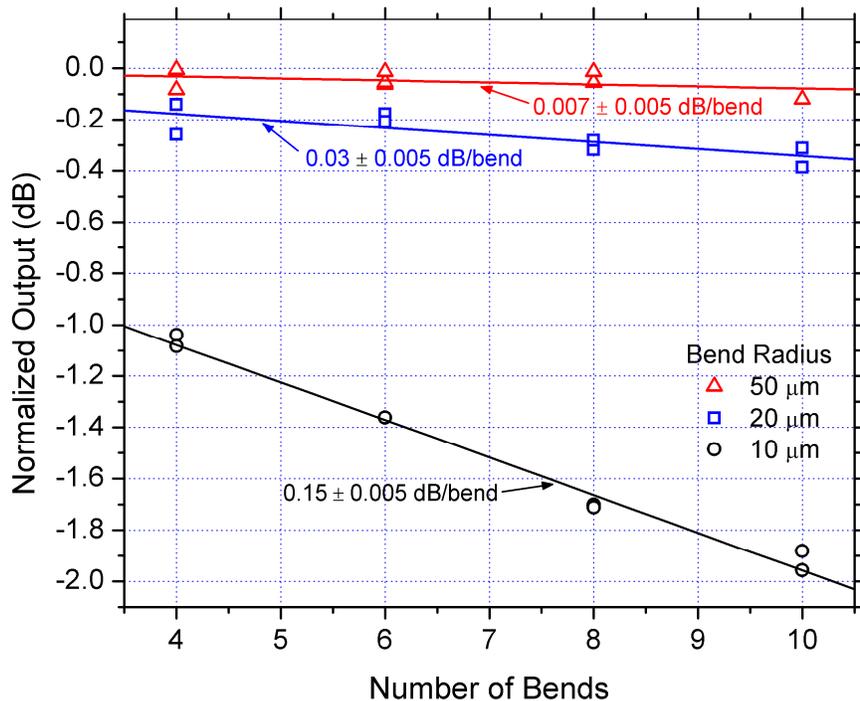


Fig. 6. Measured bend loss as a function of bend radius for 1  $\mu\text{m}$  wide etchless waveguides. Bending losses are negligible for bends as small as 50  $\mu\text{m}$ . The output is normalized relative to -13.6 dBm.

In summary, we fabricated a low confinement etchless silicon waveguide with losses of 0.3 dB/cm. Etchless waveguides can achieve bending radii of 50  $\mu\text{m}$  and thus, enable higher integration than ridge waveguides with similar losses. Thicker etchless waveguides can be fabricated using thermal oxidation to achieve even smaller bending radii.

#### Acknowledgments

The authors would like to thank John R. Lowell from Defense Advanced Research Projects Agency (DARPA) for supporting this work under the DARPA Optical Arbitrary Waveform Generation Program and the DARPA Slow-Light Program. This work was performed in part at the Cornell NanoScale Facility, a member of the National Nanotechnology Infrastructure Network, which is supported by the National Science Foundation (Grant ECS-0335765). The authors would also like to thank Christina Manolatou for her finite difference mode solver, and Bradley Schmidt and Robert J. Meyers for useful discussions.