4 × 44 Gb/s Packet-Level Switching in a Second-Order Microring Switch

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Abstract—We demonstrate simultaneous switching of wavelength-division-multiplexed (WDM) data consisting of four 44-Gb/s channels (176 Gb/s total) through an electro-optically active second-order microring switch with a 0.7-ns rise and a 3.4-ns fall time. The higher order microring device allows fast simultaneous switching of multiple high data rate WDM channels. We verify the correct active switching operation and low resultant power penalties on both switch output ports. The ability to switch multiple high data rate channels simultaneously at high speed with low power consumption makes higher order ring switches attractive components for silicon photonic switching fabrics.

Index Terms—Microring switch, photonic interconnection networks, wavelength-division-multiplexed (WDM).

I. INTRODUCTION

SILICON photonic based optical interconnects have been proposed as a possible solution to communication bottlenecks in today's high-performance computing systems. In such optical interconnects, microring resonator devices made on the silicon on insulator (SOI) platform are promising components due to their compact size, complementary metal-oxide semiconductor (CMOS) process compatibility, and power efficiency. A variety of network on chip (NoC) architectures has been proposed to use microring resonators to increase bandwidth and power efficiency in both inter-core and memory access [1]–[4].

A common assumption in these architectures is the ability to send large amounts of data through the microrings by leveraging WDM. Previous demonstrations have shown the ability to switch a large number of channels through optically pumped [5] and thermally tuned [6] microring devices.

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However, thermal tuning cannot easily achieve nanosecond scale switching offered by EO active microring switches and optically pumped switching is neither power efficient nor easily feasible. Other WDM capable fast devices such as Mach–Zehnder Interferometer (MZI) switches are attractive for their performance but require a much larger footprint which might be problematic for dense NoCs [7].

The first demonstration of using a second-order EO microring resonator switch is in [8] at 10 Gb/s, and subsequent demonstrations consisted of three channels of 10 Gb/s data [9], or a single channel of 40 Gb/s data [10]. This letter is the first demonstration of high bitrate WDM operation on an EO microring switch.

II. DEVICE CHARACTERIZATION

The device used in this experiment is a second-order 1×2 switch consisting of two cascaded microrings coupled to two adjacent waveguides. The device was fabricated at the Cornell Nanofabrication Facility, and a detailed characterization can be found in [11].

Electrical carriers can be injected into both of the rings via separate PIN diodes to tune the resonance of the device. This resonance shift allows optical signals to be switched to the drop port when on-resonance, and the through port when off-resonance. Fig. 1 shows an spectrum scan of the device during the passive state, where no electrical carriers are injected. The free spectral range (FSR) of the device is 9.1 nm, and through-port 3 dB passband bandwidth is 70 GHz. The passbands of the two cavities are not perfectly overlapping in the passive state, but are aligned during active switching. Single channel dynamic extinction ratio greater than 20 dB is possible [11].

The resonance locations allow us to switch four wavelength channels inside the C-band with this device. We place the channels so that they are switched to the drop port when a voltage bias is applied, and the wavelengths are optimized to balance the extinction ratio between the two ports at each channel. A CMOS compatible square wave having amplitude 0.95 V, 0 V DC bias, 100 ns period, and 50% duty cycle drives the switch to send periodic data to both output ports (Fig. 2(a)).

The applied voltage also changes the FSR of the device, thus the absolute resonance shift is different for each channel. A trade-off must be made between higher extinction ratio at any one channel and balanced performance on all channels. This trade-off is more pronounced for higher order devices
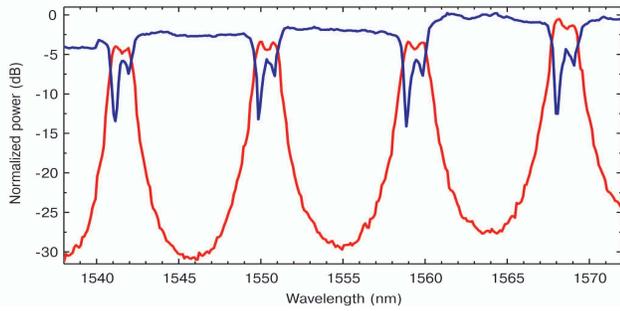
Fig. 1. Spectral scan of the device during passive state for through port (red) and drop port (blue).
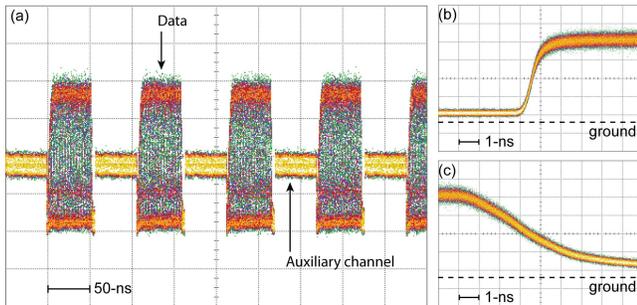

Fig. 2. (a) Signal seen by the receiver. Periodic data are combined with an auxiliary channel to maintain a constant average power over each 100 ns period. (b) and (c) Rise and fall waveforms at the start and end of the data packet, showing the speed of the microring switch.

TABLE I
DYNAMIC SWITCHING EXTINCTION RATIO

Channel λ (nm)	Through port (dB)	Drop port (dB)
1540.06	8.2	9.5
1548.87	8.4	8.7
1557.92	9.0	8.9
1567.03	8.9	8.5

because it is more difficult to line up the multiple resonances at every channel.

Table I shows dynamic extinction ratios achieved for each of the channels. These ratios are lower than the static extinction ratios due to the above mentioned trade-off, but perhaps can be improved by customizing the RF driving signal. The rise and fall times for the four switched channels, from 20% to 80%, are similar at 0.7 and 3.4 ns respectively (Fig. 2(b) and (c)). The fall time is significantly longer than the rise time due to carrier injection being faster than carrier depletion, which is related to the nanosecond lifetimes of carriers in the device. The fall time can be minimized by applying pre-emphasis [12].

III. EXPERIMENT

The experimental setup is shown in Fig. 3. Four CW lightwaves are generated by tunable laser sources. They are combined by a 4-to-1 combiner and are aligned to the same polarization. The combined signal is modulated using a commercial Mach–Zehnder modulator driven by a 44 Gb/s, $2^{15}-1$
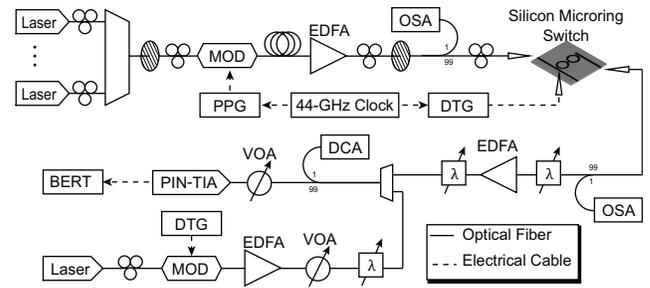

Fig. 3. Experimental setup.

pseudorandom bit sequence (PRBS) pattern created by a pulse pattern generator (PPG).

The signal is decorrelated, amplified, and then coupled onto the chip using tapered fiber. The signal on chip has quasi-TM polarization to obtain the best extinction ratio. The switch is driven by a data timing generator (DTG), which contacts the silicon chip with two sets of 20 Ghz bandwidth RF probes.

The total average power launching onto the chip is 10.6 dBm, and power levels per channel are equalized so that the the power recovered (filter and amplified one at a time) is the same for all channels. The recovered signal is received by a photodetector (PIN-TIA) and evaluated by a bit-error rate tester (BERT). Eye diagrams are recorded using a digital communications analyzer (DCA).

An auxiliary channel is added before detection to maintain a constant average power entering the AC coupled receiver setup. The auxiliary channel is arbitrarily generated at 1555 nm, and is modulated by the DTG so that it is present during the empty 50 ns parts of the data packet stream (Fig. 2(a)). Its amplitude is adjusted to match the data eye crossing level.

All the clock sources are synchronized and the DTG gates the BERT to measure the packets only when they are valid and free from rise and fall transients. This gating amounts to 41 ns measured out of each 50 ns packet, also accounting for setup time of the BERT.

For back-to-back we replace the chip with a variable optical attenuator (VOA), and match the insertion loss at each channel. The auxiliary channel is not added. To account for the 50% duty cycle data stream we reduce attenuation by 3 dB, but due to imperfect extinction the exact attenuation reduction needed is less than 3 dB. This difference does not significantly affect the final power penalty because the EDFA amplification is not sensitive to small changes in input power in our operating regime. A calibration places this effect on power penalty as negligible for the through ports and at most 0.2 dB better for drop ports.

IV. RESULTS

Figs. 4 and 5 show BER measurements for each channel at both ports, along with the back-to-back measurements for each channel. Error-free operation, defined as having BER less than 10^{-12}, is achieved for all channels. Table II lists the power penalties for each channel at 10^{-9} BER.
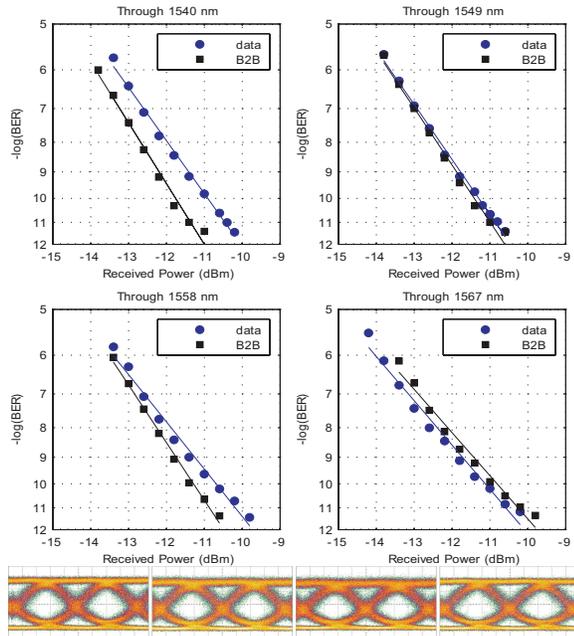
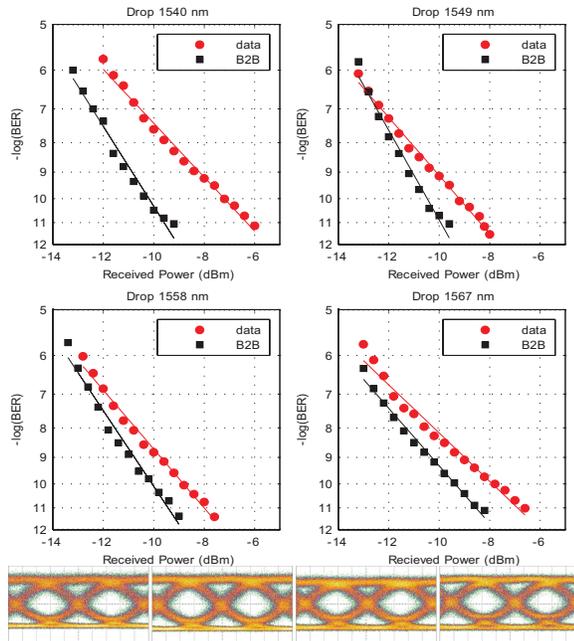Fig. 4. Through port BER curves and eye diagrams in channel order.

Fig. 5. Drop port BER curves and eye diagrams in channel order.

For the through port, power penalties are small except for the 1540 nm channel. The degradation seen at this channel is probably caused by wavelength dependent performance of the EDFA coupled with suboptimal spectral response of the device at this wavelength. The small negative penalty seen in the 1567 nm channel is likely due to experimental variation. For the drop port, power penalties are larger, again with the 1540 nm channel showing the worst behavior. The larger power penalty seen in the drop port is likely caused by spectral filtering effects from the microring [9].

TABLE II
POWER PENALTIES MEASURED AT 10^{-9} POINT

Channel λ (nm)	Through port (dB)	Drop port (dB)
1540.06	1.1	2.5
1548.87	0.1	1.0
1557.92	0.5	1.0
1567.03	−0.3	1.5

V. CONCLUSION

We demonstrate record data rate simultaneous nanosecond switching of WDM signal through a second-order microring switch, and verify error free operation for all channels. We achieve near uniform switching performance on all channels by balancing single and multichannel performance.

Future devices can be made with larger ring diameters and lower FSR values. Such devices can switch more wavelength channels, and when combined with integrated high-speed electronics, achieve even higher per-channel data rates. They can thus enable extremely efficient optical switching in future silicon-photonic based NoCs. The optimization in multichannel performance in these higher-order switches still needs to be investigated.

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