

Scalable 3D dense integration of photonics on bulk silicon

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Abstract: We experimentally show vertically stacked, multi-layer, low-temperature deposited photonics for integration on processed microelectronics. Waveguides, microrings, and crossings are fabricated out of 400°C PECVD Si₃N₄ and SiO₂ in a two layer configuration. Waveguide losses of ~1 dB/cm in the L-band are demonstrated using standard processing and without post-deposition annealing, along with vertically separated intersections showing -0.04 ± 0.002 dB/cross. Finally 3D drop rings are shown with 25 GHz channels and 24 dB extinction ratio.

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1. Introduction

Advances in silicon and silicon-compatible photonics have spurred intense research in the area of optical interconnects, where it could potentially be used to increase the bandwidth and lower the power of computing systems such as multi- and many-core processors [1,2]. However optical interconnects might need to provide not just one optical Wavelength Division Multiplexing (WDM) link, but many in order to provide enough performance gain in terms of bandwidth and power to surpass the multi-Tbps electric interconnects now in use in recent multi-core processors [3]. Researchers have already published work which shows optical networks winning against electronic ones, but only when provided with enough WDM channels [4–6]. Waveguide crossings, for example, are a necessary limitation of single layer optical networks, and are often cited as one of the biggest obstacles in these systems [7,8]. A multilayered system could reduce or eliminate these restrictions by avoiding physical crossings as well as avoid the traditional limitations of limited real estate on a chip. Multiplayer photonics would also provide architects a new dimension to explore; opening the door to denser as well as more complex networks with radically higher cross-sectional bandwidth and reduced communication power consumption. Figure 1 shows a vision of a 3D optical network comprising of several photonic layers above an electronics die.

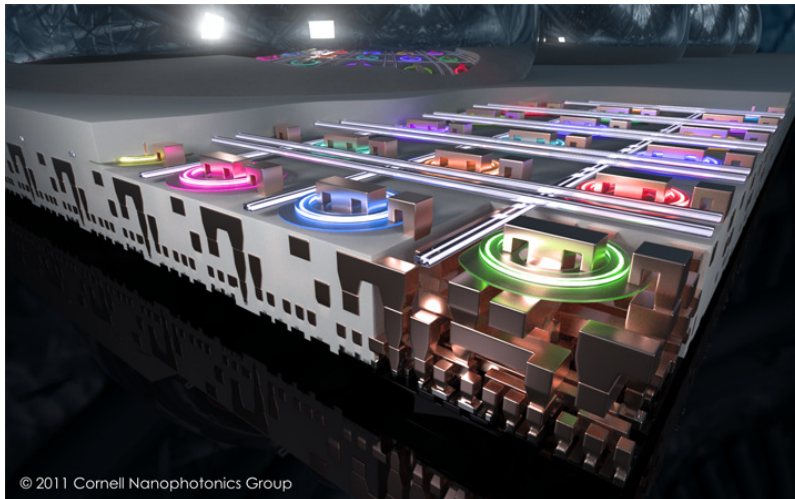


Fig. 1. Vision of a 3D optical network on a microelectronic chip based on deposited optics over CMOS electronics. Multiple bus waveguides are positioned at different vertical layers above a set of an array of microring resonators.

There is a second reason why densely integrated silicon photonics with microelectronics has yet to emerge commercially. While there may be clear advantages over electronic communication, the integration of photonic interconnects with on-chip electronics requires a costly change to well-established Complimentary Metal-Oxide-Semiconductor (CMOS) processes. Research groups often rely on a Silicon-on-Insulator (SOI) stack with a guiding medium of single-crystal silicon (c-Si) above several micrometers of optically insulating silica (SiO_2). While the materials are directly compatible (unlike III-V materials) the c-Si must still be grown independently, implanted, annealed, cut, oxidized and bonded to another structural Si wafer before it can be used for device fabrication. Besides difficult and costly, this approach limits photonics to a single layer. In addition using this c-Si for both electronics and photonics is problematic since photonics requires a thick oxide layer (typically a few micrometers) underneath for optical isolation while SOI electronics requires a small layer of only tens to a few hundred nanometers in order to ensure thermal flow from the devices to the substrate. Research groups, including ours have shown that this layer can be repurposed for optics [9,10], however generally at the cost of more real estate and with some modification of standard fabrication.

2. Photonic Materials for Back-End Integration

Using deposited photonic materials in a back-end process could enable the integration of photonics with microelectronics without suffering from the above limitations. Along with using group IV compatible materials, back-end process requires deposition and processing of materials around or below 400°C to avoid distressing the metallization and changing the dopant diffusion. Our fabrication is then governed by plasma enhanced chemical vapor deposition (PECVD) of all layers, planarization to allow for vertical stacking, and proper patterning and spacing of structures to allow for coupling and insulation. Regarding materials one needs a set of two with an appreciable refractive index ratio to keep bends and inter-waveguide spacing small. Silica is commonly used as an outer cladding layer as it has a fairly low refractive index of around 1.45 at telecom wavelengths ($\sim 1.55 \mu\text{m}$), and it is found in abundance in CMOS. For active devices such as modulators, detectors and switches, one could rely on polymeric materials [11], polycrystalline silicon (p-Si) [12], hydrogenated amorphous silicon (a-Si:H) [13], or poly-germanium (poly-Ge) [14]. For passive device some

common waveguide materials include silicon nitride (Si_3N_4) [15,16] and amorphous silicon (a-Si) [17,18] as low optical loss waveguides.

Table 1. CNF GSI PECVD Material Recipes

| | Si_3N_4 | SiO_2 |
|--|-------------------------|-------------------------------|
| Gas 1 (sccm) | 28 (SiH_2) | 18 (SiH_2) |
| Gas 2 (sccm) | 1900 (NH_3) | 1800 (N_2O) |
| RF Power at 13.56 MHz (W) | 350 | 100 |
| Temperature ($^\circ\text{C}$) | 400 | 400 |
| Pressure (Torr) | 3.5 | 1.4 |

Here we show a passive multilayer WDM optical link made from CMOS back-end compatible materials and process. We chose to work with Si_3N_4 as a guiding medium for its good optical characteristics. Silicon nitride is readily found in CMOS for passivation, masking and dielectric layers [19] and provides lower optical losses than c-Si in the NIR [20,21] when using SiO_2 cladding, also a CMOS dielectric. Low pressure chemical vapor deposition (LPCVD) silicon nitride has been shown to have losses as low as 0.1 dB/cm [22]. Unfortunately in PECVD the losses increase with added impurities; specifically we expect absorption of Si-H and N-H bonds centered on $\lambda = 1.5 \mu\text{m}$. We explored a variety of PECVD recipes to reduce potential losses. One group suggests adding helium into the plasma to mitigate the hydrogen bonding environment [23]. Others yet utilize the lower frequency options of the PECVD tool to reduce bombardment of lower weight hydrogen atoms [15,24]. While preliminary testing did see some overall improvements in some of these cases of ~1-2 dB/cm the tradeoff was often extensive non-uniformity in thickness over a full 100 mm wafer, on the order of 100 nm center to edge. While these numbers are specific to the PECVD tool at the Cornell NanoScale Facility, we include here in Table 1 the details of the two final materials used in this work.

3. Fabrication

The full process starting with a blank silicon wafer can be described as 9 independent steps. We begin with a 100 mm silicon wafer, on which 3 μm of PECVD SiO_2 is deposited to provide the bottom optical insulation, shown in Fig. 2a. We deposit PECVD Si_3N_4 on this layer (Fig. 2b) using the recipe given in Table 1e pattern bus waveguides and laterally-coupled microring resonators into this layer using i-line photolithography (Fig. 2c). We term this layer “L1”, or the first photonic layer. We clad this first optical layer with PECVD SiO_2 . The conformal process creates a ridge above all nitride features (Fig. 2d). These “bumps” limit the ability to stack vertical layers, so the wafer is planarized to the waveguide level using a chemical mechanical polishing (CMP) tool and a KOH and silica solution (Fig. 2e). A second deposition of PECVD SiO_2 creates the vertical gap between optical layers, and can be used to increase or reduce coupling between these (Fig. 2f). Adjusting the gap, and therefore the coupling by deposition gives us considerably more control than the typical lateral coupling, which is dependent on resist, lithography and etching limitations. The second Si_3N_4 layer is then deposited and patterned the same way as the first (Fig. 2g-h). We term this layer “L2”, the second photonic layer. Finally we clad again in PECVD SiO_2 , again for 3 μm as a final insulation layer (Fig. 2i).

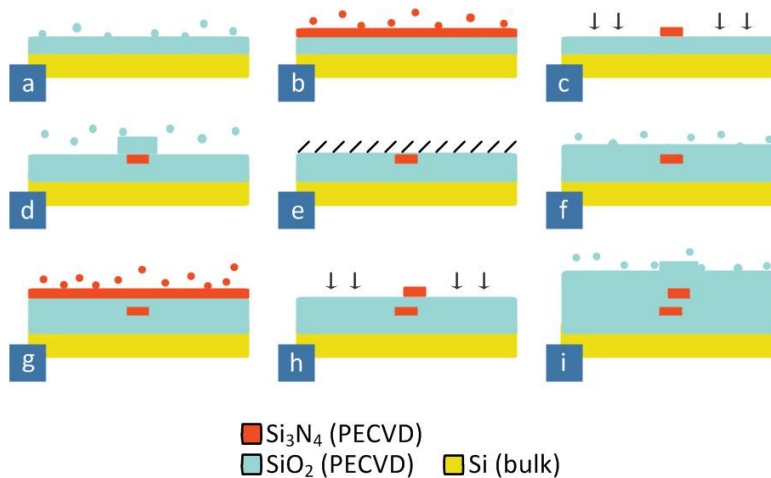


Fig. 2. Fabrication of a 2-layer optical link: (a) deposit SiO₂ as BOX; (b) deposit Si₃N₄ for first guiding layer; (c) pattern/etch L1 waveguides and rings; (d) deposit SiO₂ for lateral buffer; (e) polish and planarize SiO₂ layer with CMP; (f) deposit SiO₂ as spacer; (g) deposit Si₃N₄ for second guiding layer; (h) pattern/etch L2 waveguides; (i) deposit SiO₂ as final cladding layer.

4. Devices and Results

We fabricated a multi-layer optical link, traversing two layers and one passive WDM filter. The first layer (L1) was patterned with waveguides and rings with 30 μm radius. L1 spans the full die ending in inverse-tapered couplers [25] on both ends of the chip to provide an input and through port. L2, the second photonic layer begins above the microring resonator and extends to the output facet, where light can be coupled out to read the drop port (see Fig. 3a). The coupling between the L2 waveguides and the ring resonator is set by the vertical and horizontal offsets provided by the mid-layer SiO₂ layer and lithographic positioning shown in Fig. 3b. Figure 3c and Fig. 3d show false-color SEM images of the cross section of the chip with emphasis on the L1 waveguide.

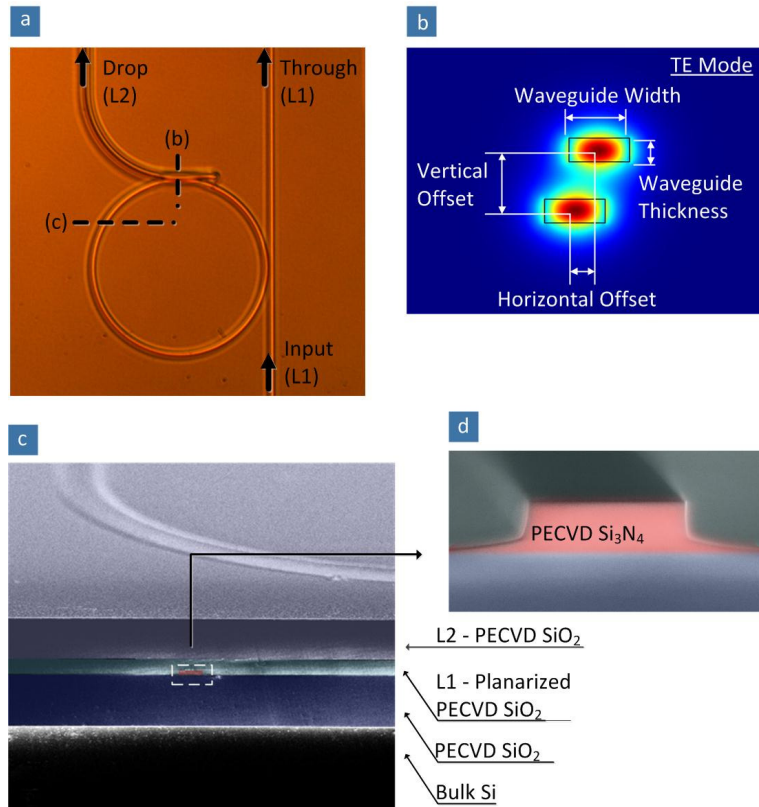


Fig. 3. (a) Microscope image of bus waveguides and microring resonator; (b) vertically coupled structure with TE mode and geometry parameters; (c) false color SEM image of ring cross section; and (d) close-up SEM of silicon nitride waveguide cross section.

Waveguide loss measurements were taken using the cut-back method, whereby we fabricated many waveguides with varying lengths in order to isolate propagation loss. We show this loss plotted as a function of distance in Fig. 4a, where we estimate it to be just over 1 dB/cm for most of the L-band in our 400 nm x 1 μ m geometry. The loss increases steadily into the C-band due to Si-H and N-H bonds in the film [16]. These losses are comparable to those shown in the literature for silicon nitride and are still better than most comparable silicon single-mode waveguides [21].

We measure losses for the waveguide crossings to be -0.04 ± 0.002 dB/cross for waveguides separated vertically by 800 nm. We tested them by incrementing overlapping waveguides in L2 corresponding to 25 independent waveguides in L1. Figure 4b shows this loss as compared to a 3D finite-difference time-domain (FDTD) simulation using perfect materials, estimating the ideal value around -0.015 dB/cross for this gap. Additional loss is to be expected from impurities in the PECVD. This number is a major improvement over single-layer silicon crossings which in theory can only approach this number [26] and could still be improved with increased layers.

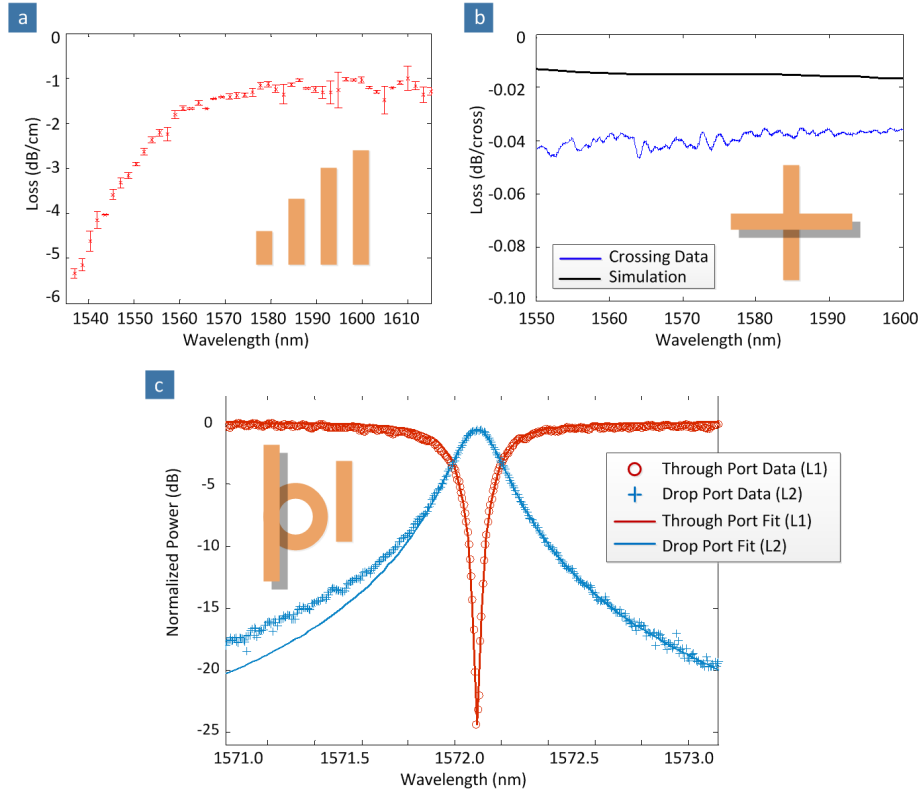


Fig. 4. Results of fabrication: (a) propagation losses of PECVD Si₃N₄ waveguides (400 nm x 1000 nm) over wavelength of interest; (b) averaged loss per vertical crossing (800 nm separation); (c) microring resonator (30 μm radius) through and drop port responses from both layers.

Lastly we test the optical path through the vertically-coupled filter and measure a channel bandwidth of 25 GHz and an extinction ratio of -24 dB. Figure 4c shows both the drop port and through port normalized by the input power to the device. We also measure an insertion loss of -0.6 dB from the drop port response, and we calculate the loaded quality factor of the resonator from the linewidth to be $Q_l = 7.5 \times 10^3$. Using temporal coupled-mode theory [27], we fit the experimental data and calculate an intrinsic quality factor greater than 10^5 for this resonator. We further validate our numbers through simulation using finite-element method (FEM) including material and bending losses from which we estimate an ideal intrinsic Q value of $Q_{i-sim} = 1.7 \times 10^5$. The spectral width is engineered for on-chip network applications in the L-Band while maintaining the critical coupling condition for high filter efficiency. These rings are considered mostly radiation limited and can be tailored to specific bandwidth values through proper coupling design.

5. Conclusion

We have demonstrated here a process for integrating multiple photonic layers on the backend of CMOS electronics. Using low-temperature PECVD Si₃N₄ as a guiding layer and PECVD SiO₂ cladding, we show multiple stacked optical layers, coupled by microring resonators, all with i-line photolithography. Furthermore we show that a major deterrent of optical networks, single-layer waveguide crossing losses, can be avoided using multiple-layer photonics. This method for fabricating on-chip optics opens the doors to a new area of optical network design

previously limited by real estate and WDM channel limitations. All processes and materials used here are compatible and common to the standard electronics CMOS process.

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